Automatic SIMDization of Parallel Sorting on x86-based Manycore Processors

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Why sorting?

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  - Databases, computational biology, graph algorithms, etc.

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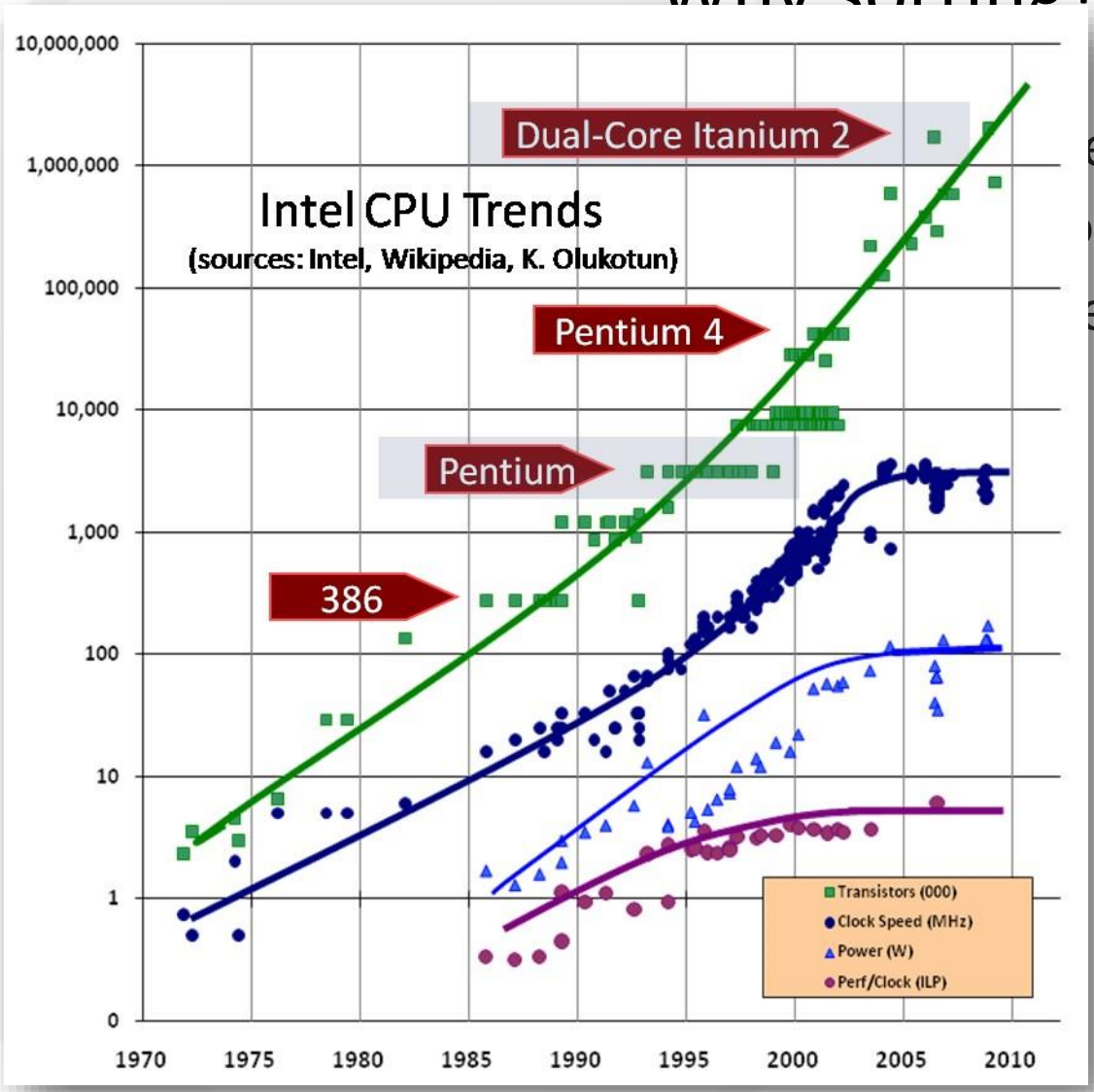

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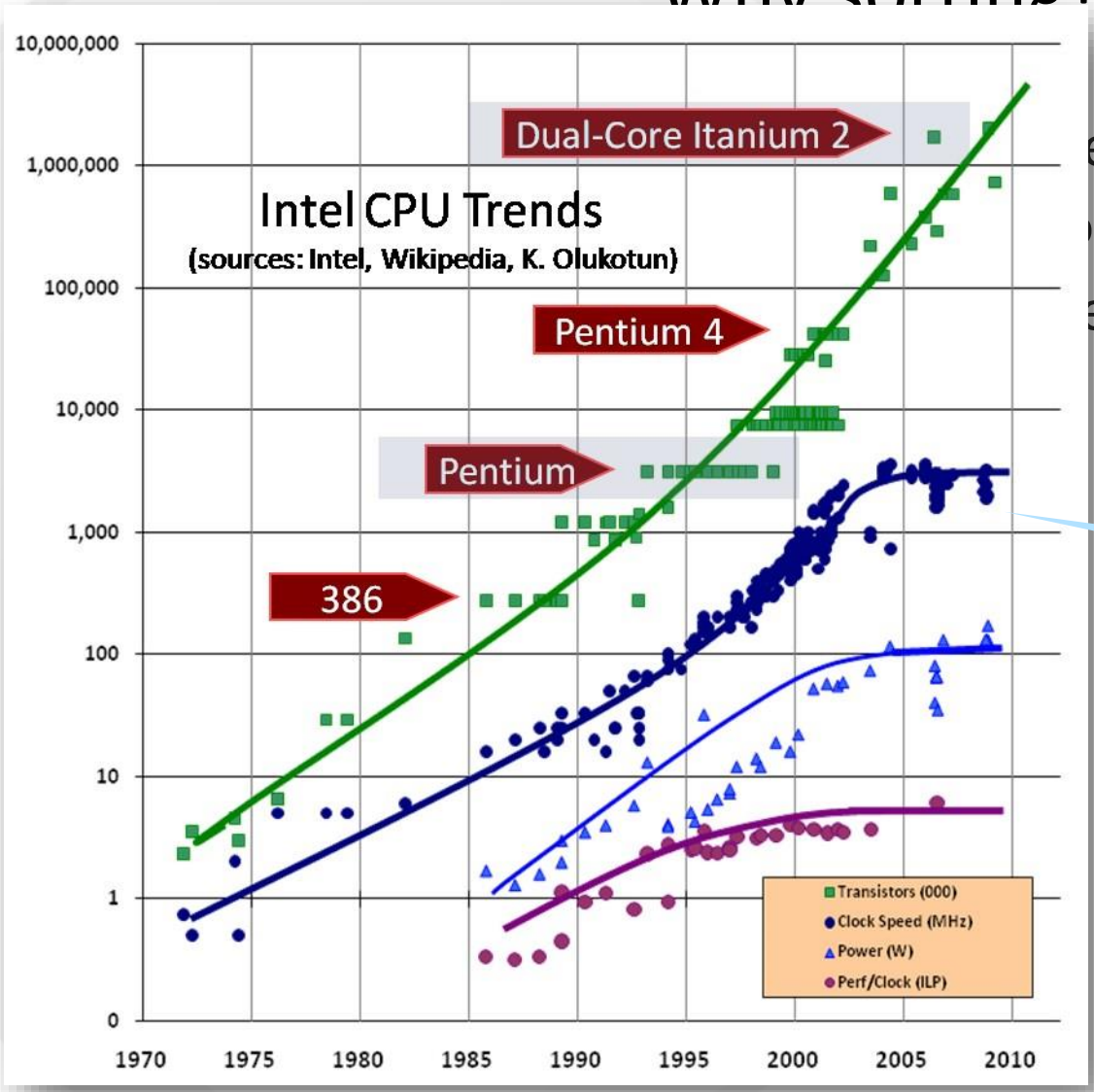

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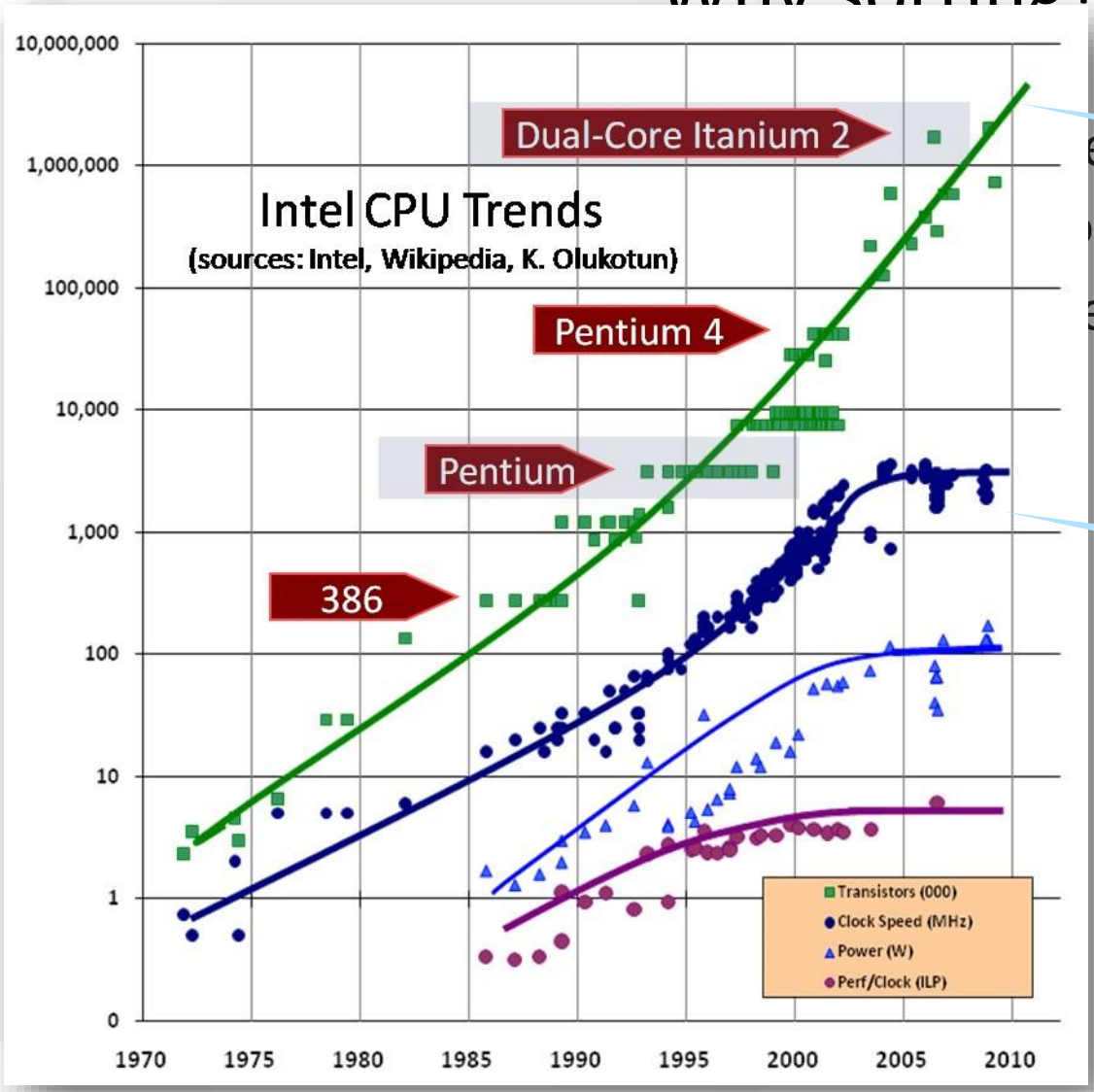

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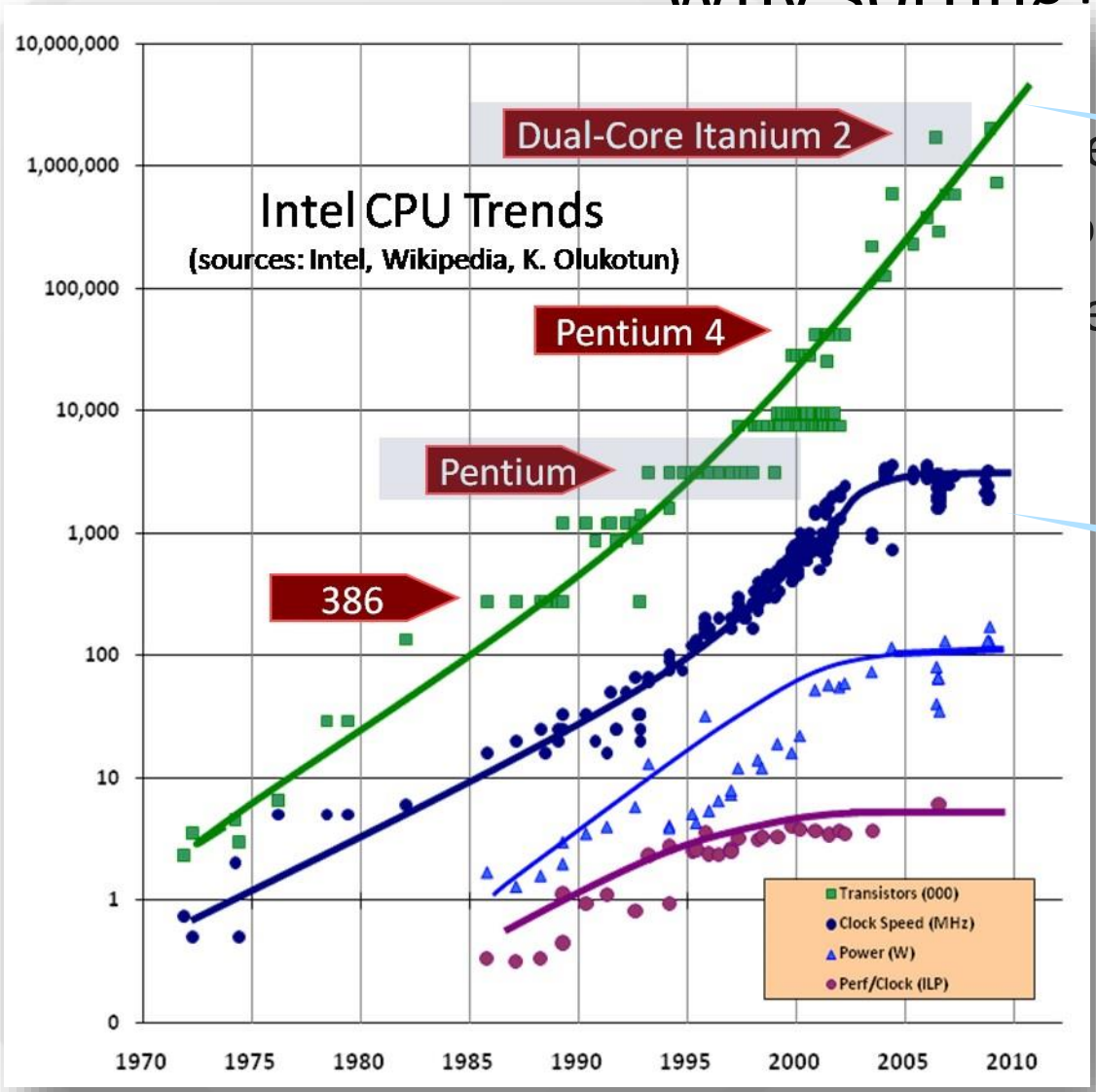

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- MIC: AVX-512 (AVX3)
  - 512-bit
  - Xeon Phi

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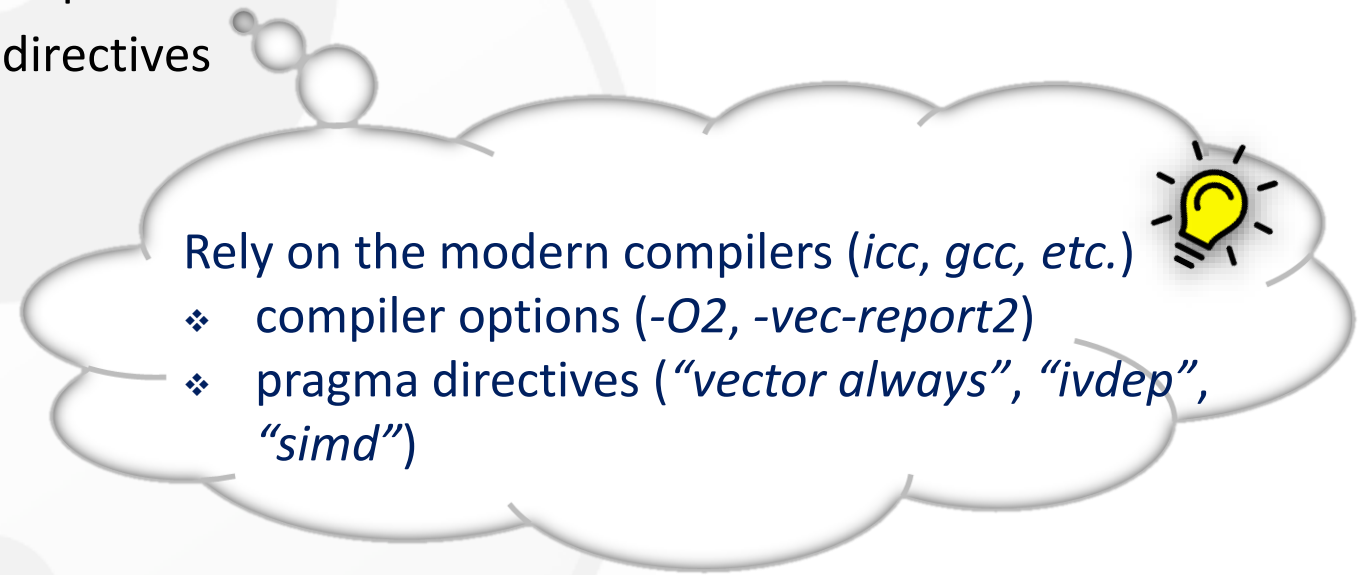

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Issues:
Fail to auto-vec loops, due to complex memory access, convoluted data rearrangement, etc.

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Tedious and error-prone.

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Serial C codes

```
for(i=0; i<2w; i++)
{
  if(i<w)
    trgA[i]= i%2!=0 ? inpB[i/2] : inpA[i/2];
  else
    trgB[i-w]= i%2!=0 ? inpB[i/2] : inpA[i/2];
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AVX intrinsics on CPUs

```
__mm256 v1 = _mm256_unpacklo_ps(inpA, inpB);
__mm256 v2 = _mm256_unpackhi_ps(inpA, inpB);
__mm256 trgA = _mm256_permute2f128_ps(v1, v2, 0x20);
__mm256 trgB = _mm256_permute2f128_ps(v1, v2, 0x31);
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AVX512 intrinsics on MIC

```
__mm512i l = _mm512_permute4f128_epi32(inpA, _MM_PERM_BDAC);
__mm512i h = _mm512_permute4f128_epi32(inpB, _MM_PERM_BDAC);
__mm512i t0  = _mm512_mask_swizzle_epi32(h, 0xcccc, l, _MM_SWIZ_REG_BADC);
__mm512i t1  = _mm512_mask_swizzle_epi32(l, 0x3333, h, _MM_SWIZ_REG_BADC);
__mm512i l = _mm512_mask_permute4f128_epi32(t1 , 0x0f0f, t0 , _MM_PERM_CDAB);
__mm512i h = _mm512_mask_permute4f128_epi32(t0 , 0xf0f0, t1 , _MM_PERM_CDAB);
__mm512i trgA = _mm512_shuffle_epi32(l, _MM_PERM_BDAC);
__mm512i trgB = _mm512_shuffle_epi32(h, _MM_PERM_BDAC);
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__mm256 v2 = _mm256_un    hi_p      inpB);
__mm256 trgA    mm256_          ps(v1     , 0x20);
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```

```
__mm512i l = _mm5                                  DAC);
__mm512i h = _mm51                                 BDAC);
__mm512i t                                         SWIZ_REG_BADC);
__mm512i t1  = _                                   WIZ_REG_BADC);
__mm512i l = _mm5                                  0f0f, t0 , _MM_PERM_CDAB);
__mm512i h = _                                     i32(t0 , 0xf0f0, t1 , _MM_PERM_CDAB);
__mm512i trgA = _mm512                             (l, _M_PERM_BDAC);
__mm512i trgB = _mm512                             ffle_epi32(h, _MM_PERM_BDAC);
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Can they be automatically generated?

ASPaS Framework

- Formalize the data-reordering patterns in the parallel sorting

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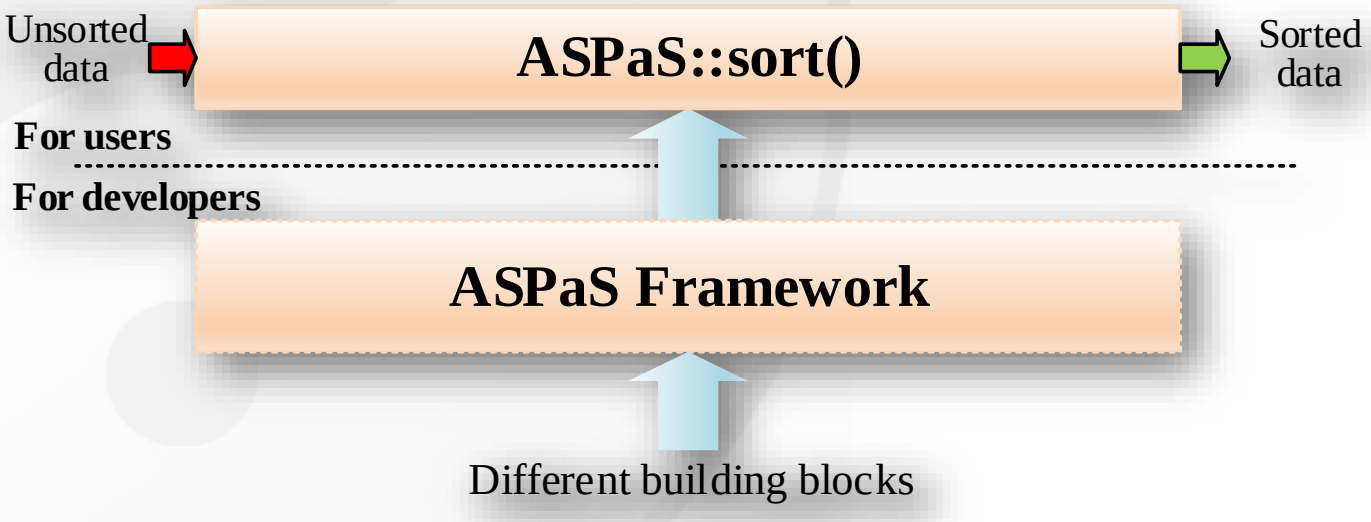

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- Introduction & Motivation
- Background
  - Sorting Networks & SIMD Processing
- ASPaS Framework
  - SIMD Sorter
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  ▷ Generate patterns for sorting the data segment by segment
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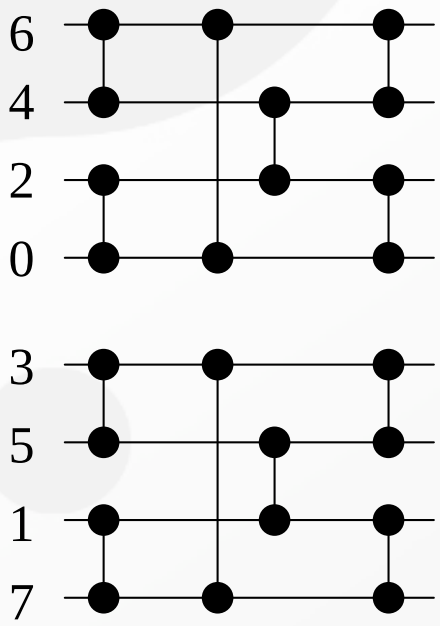

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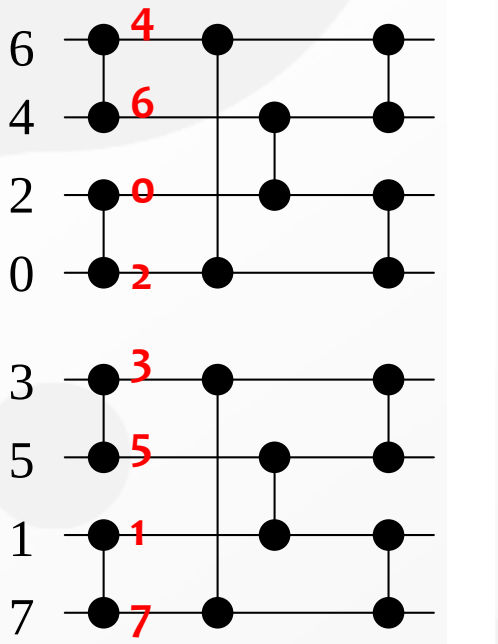

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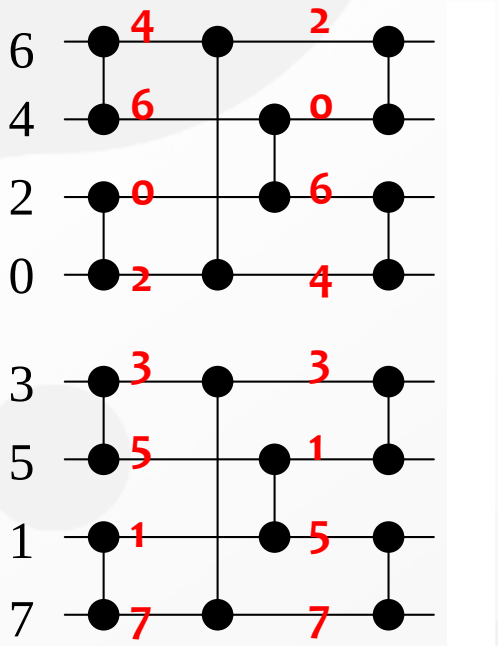

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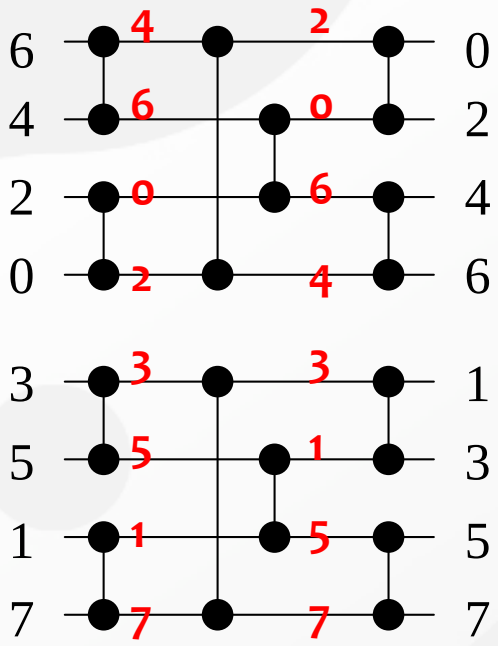

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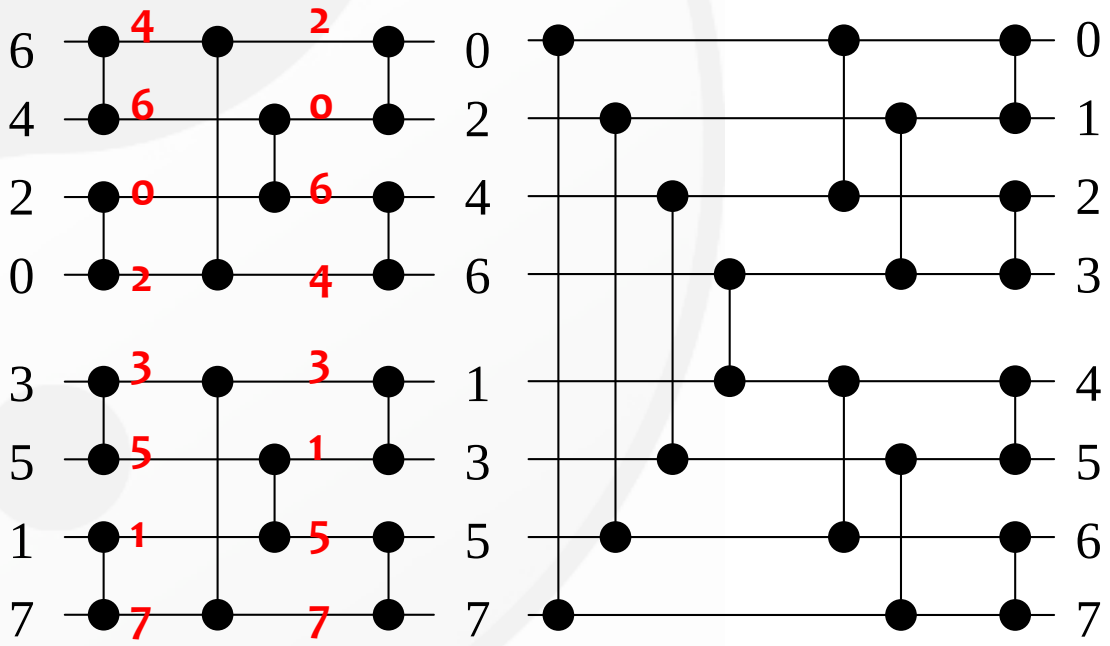

Two sorting networks Merging network

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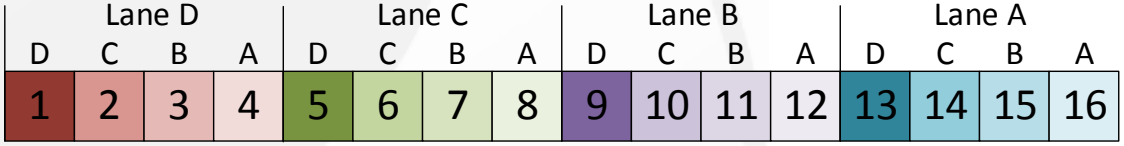

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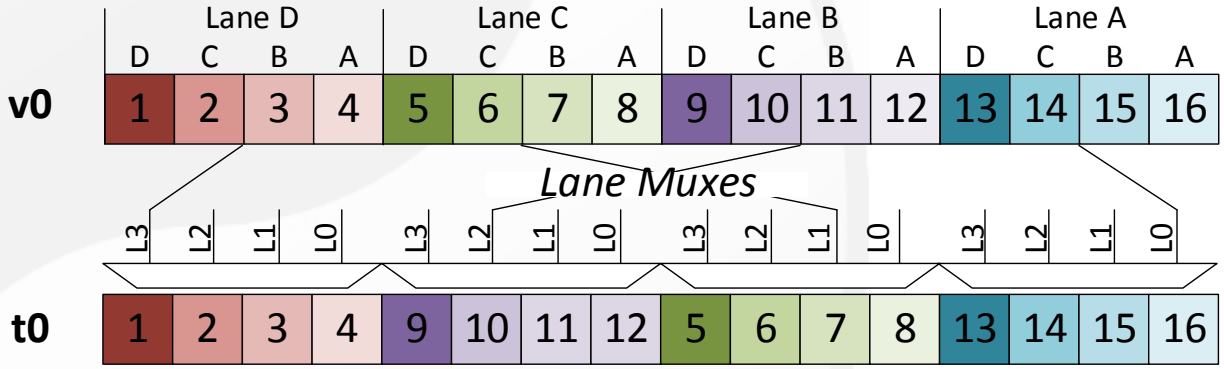

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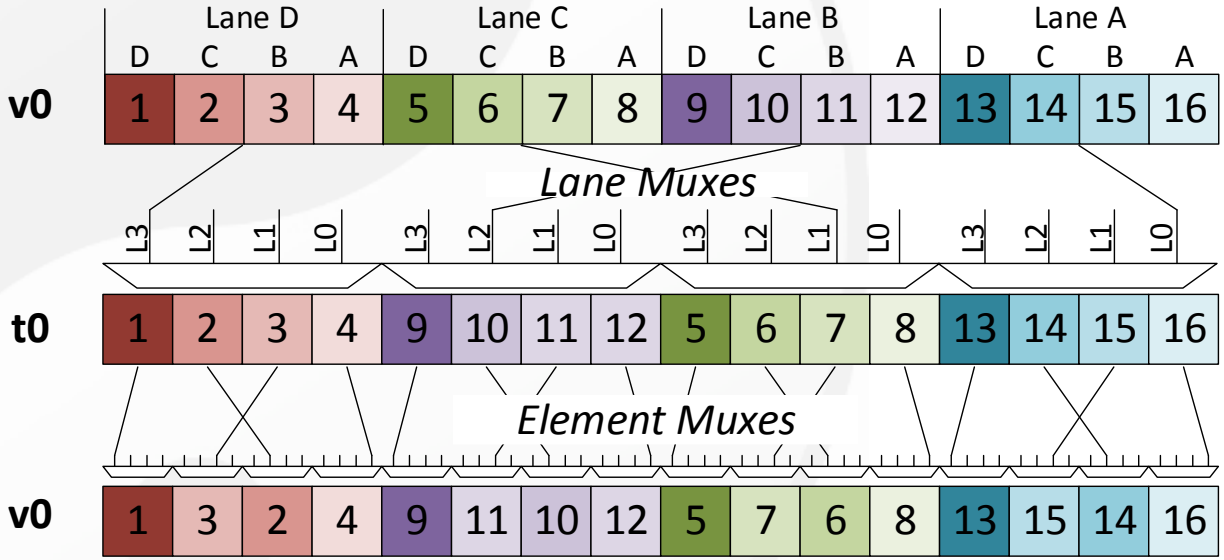

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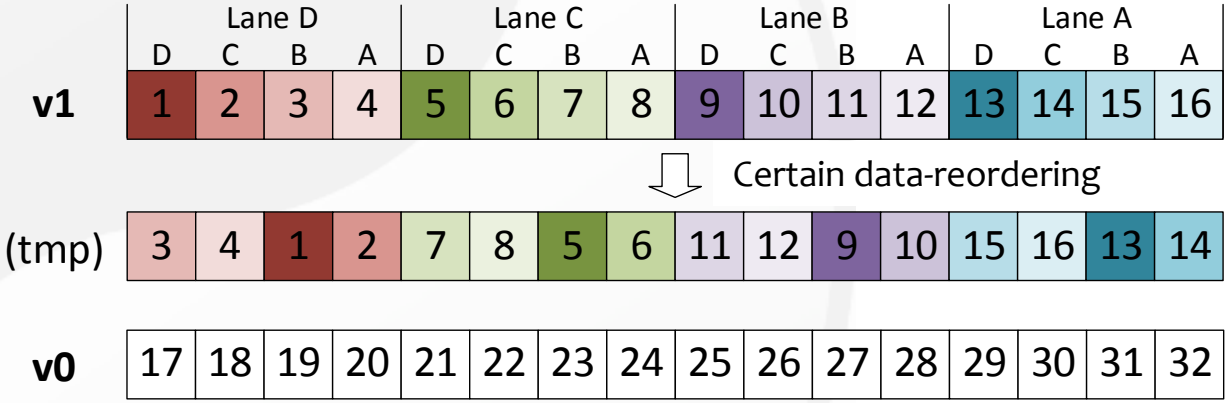

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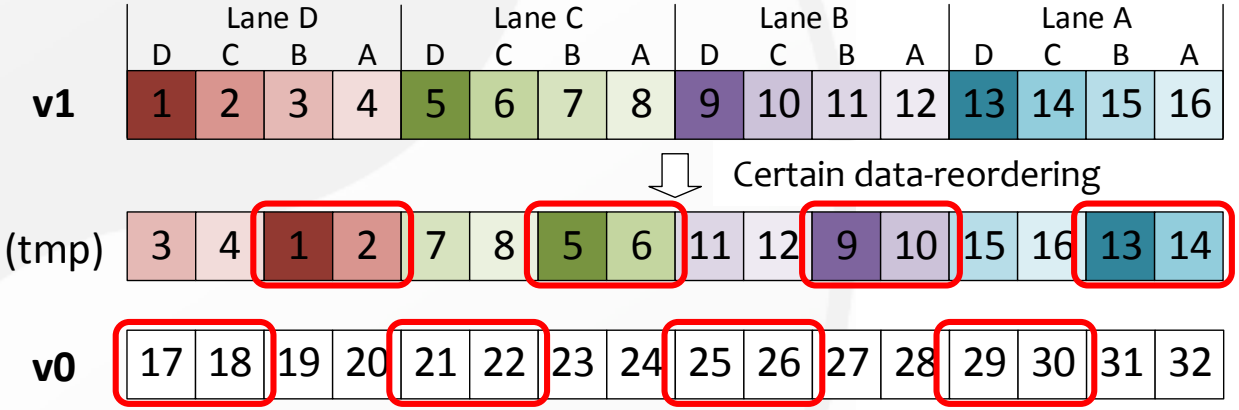

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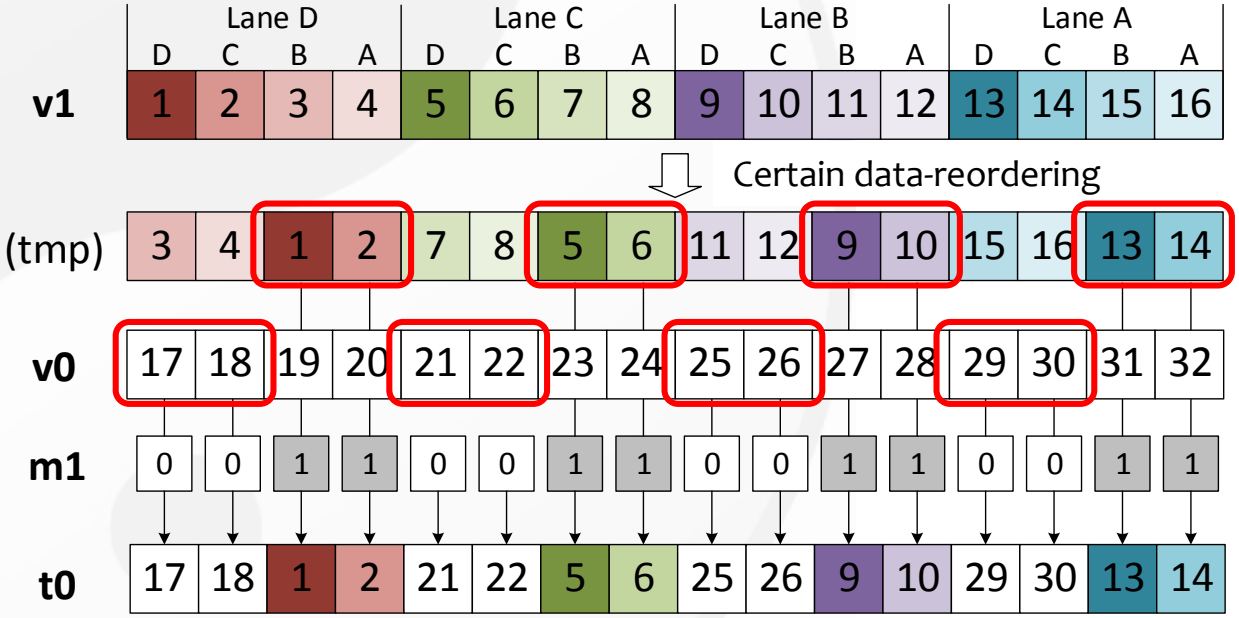

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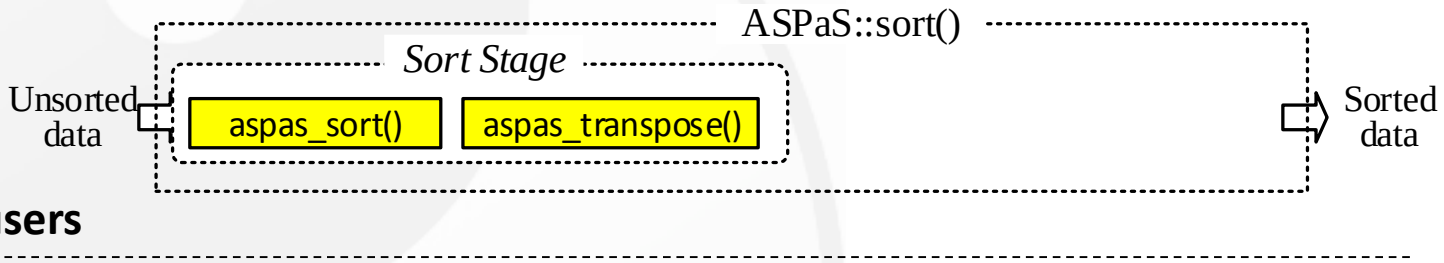

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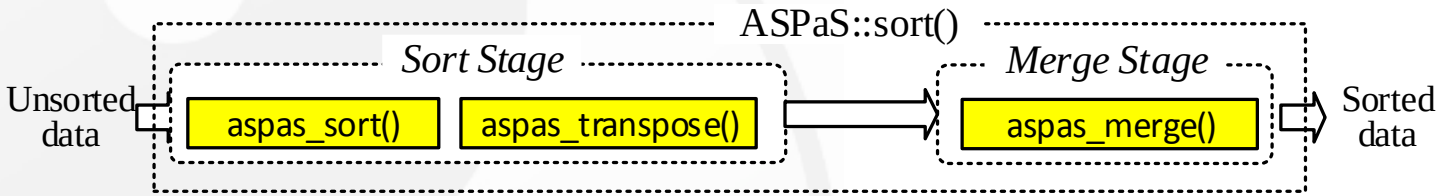

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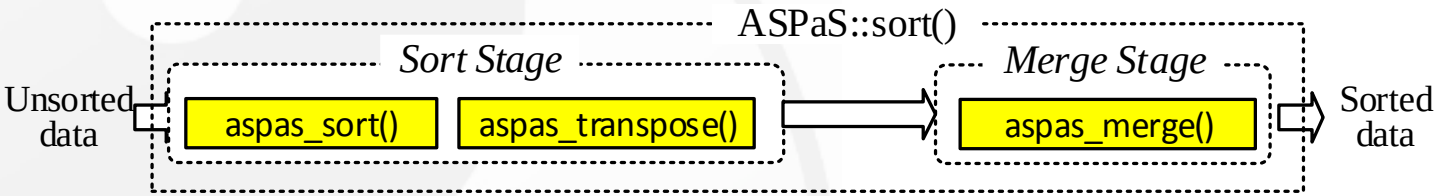

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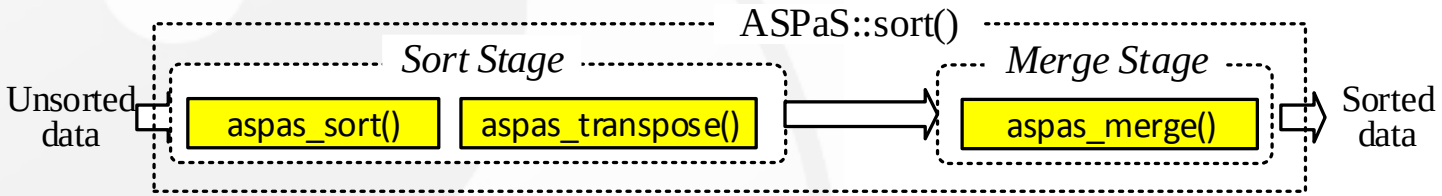

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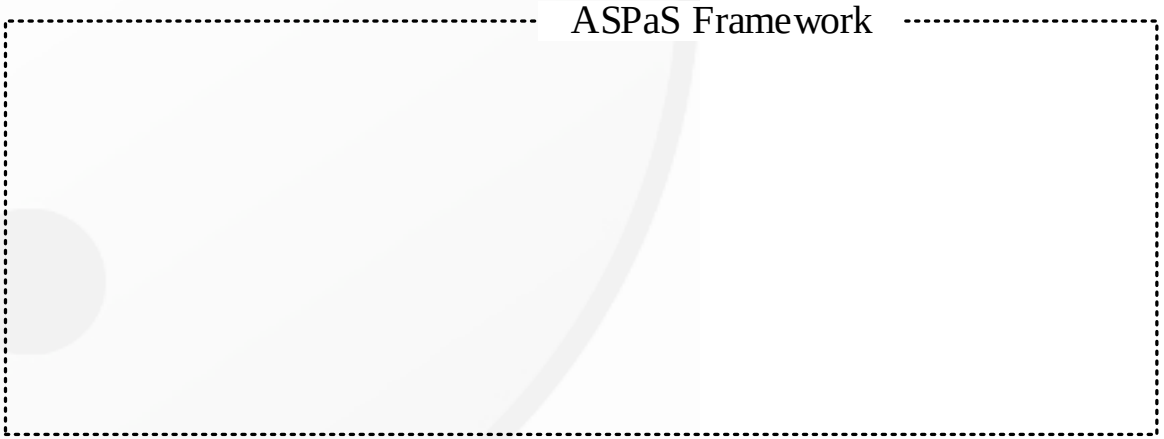

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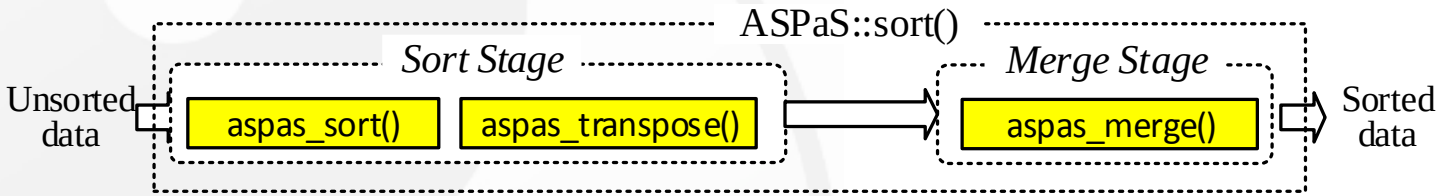

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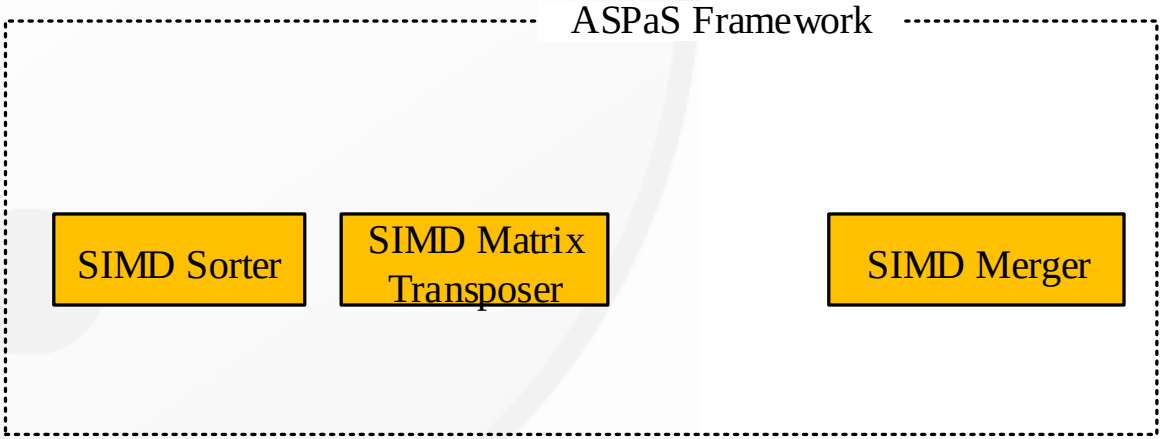

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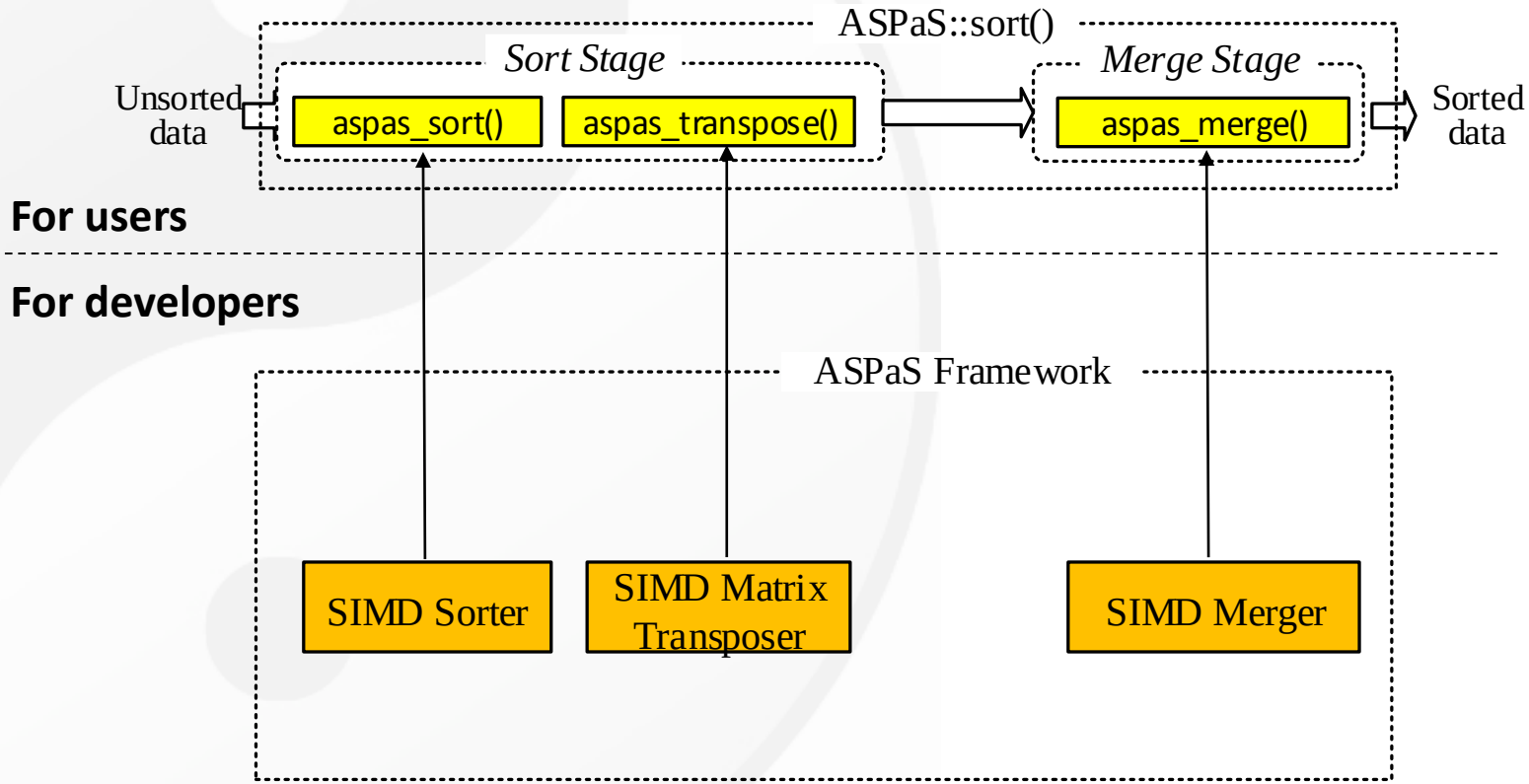

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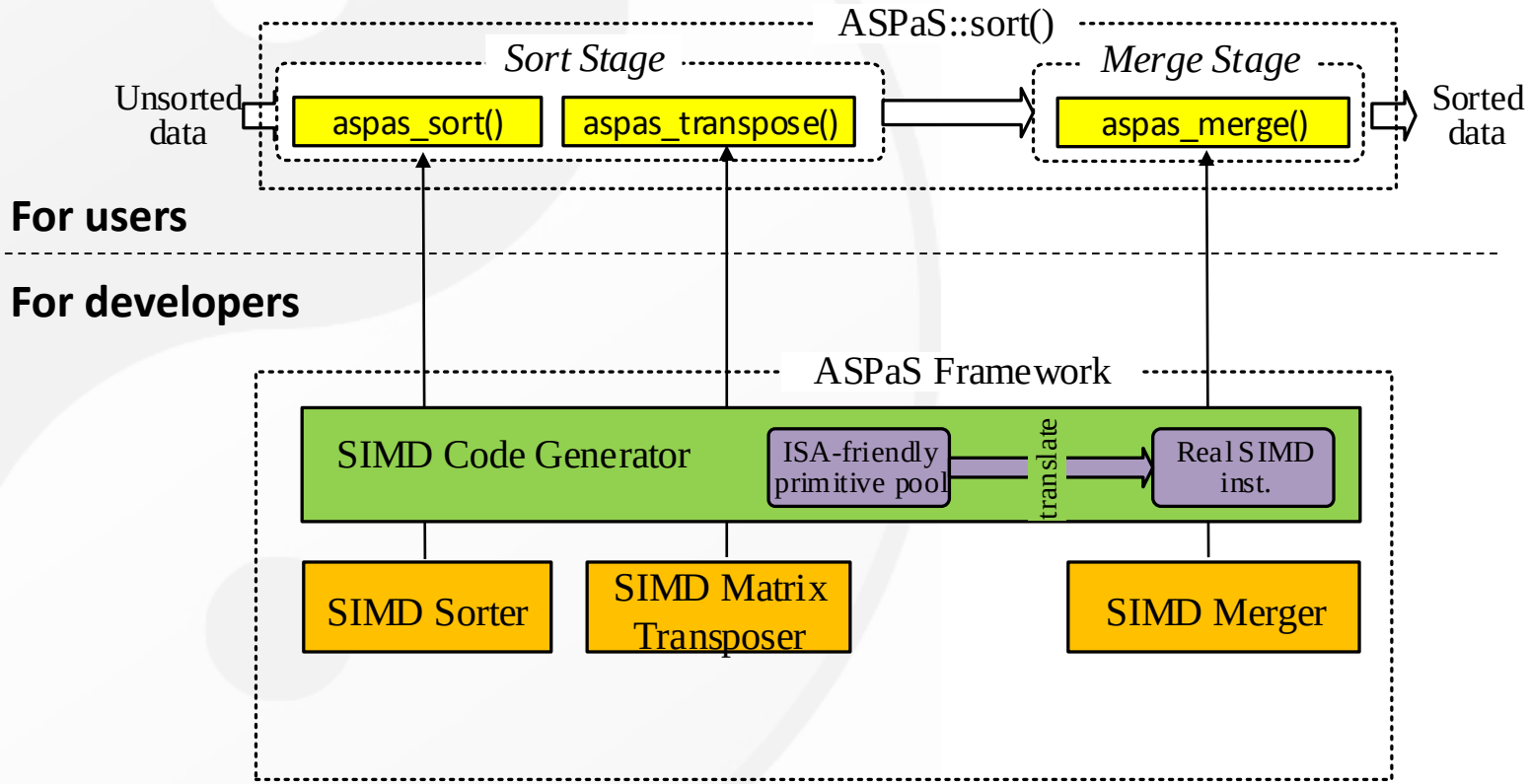

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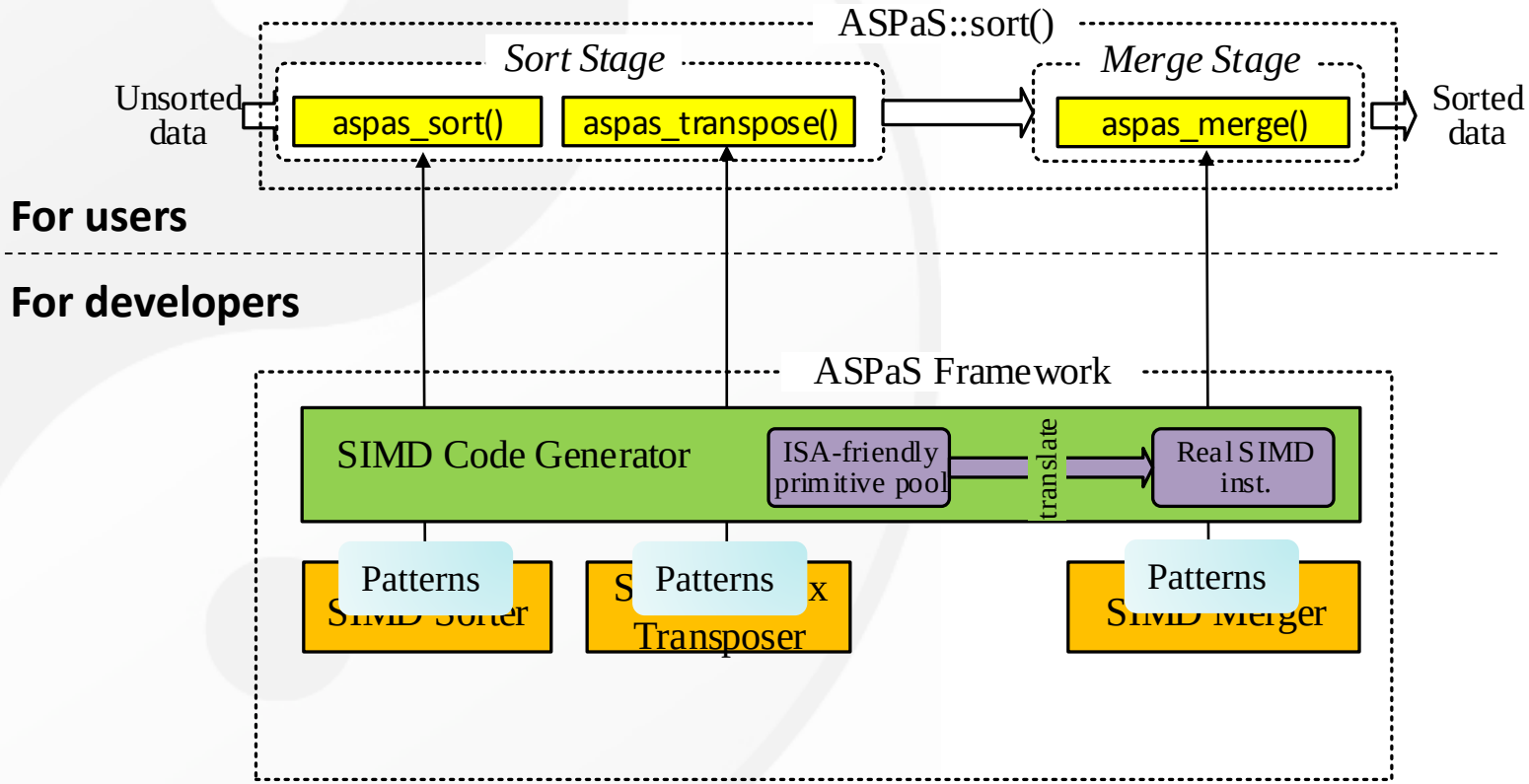

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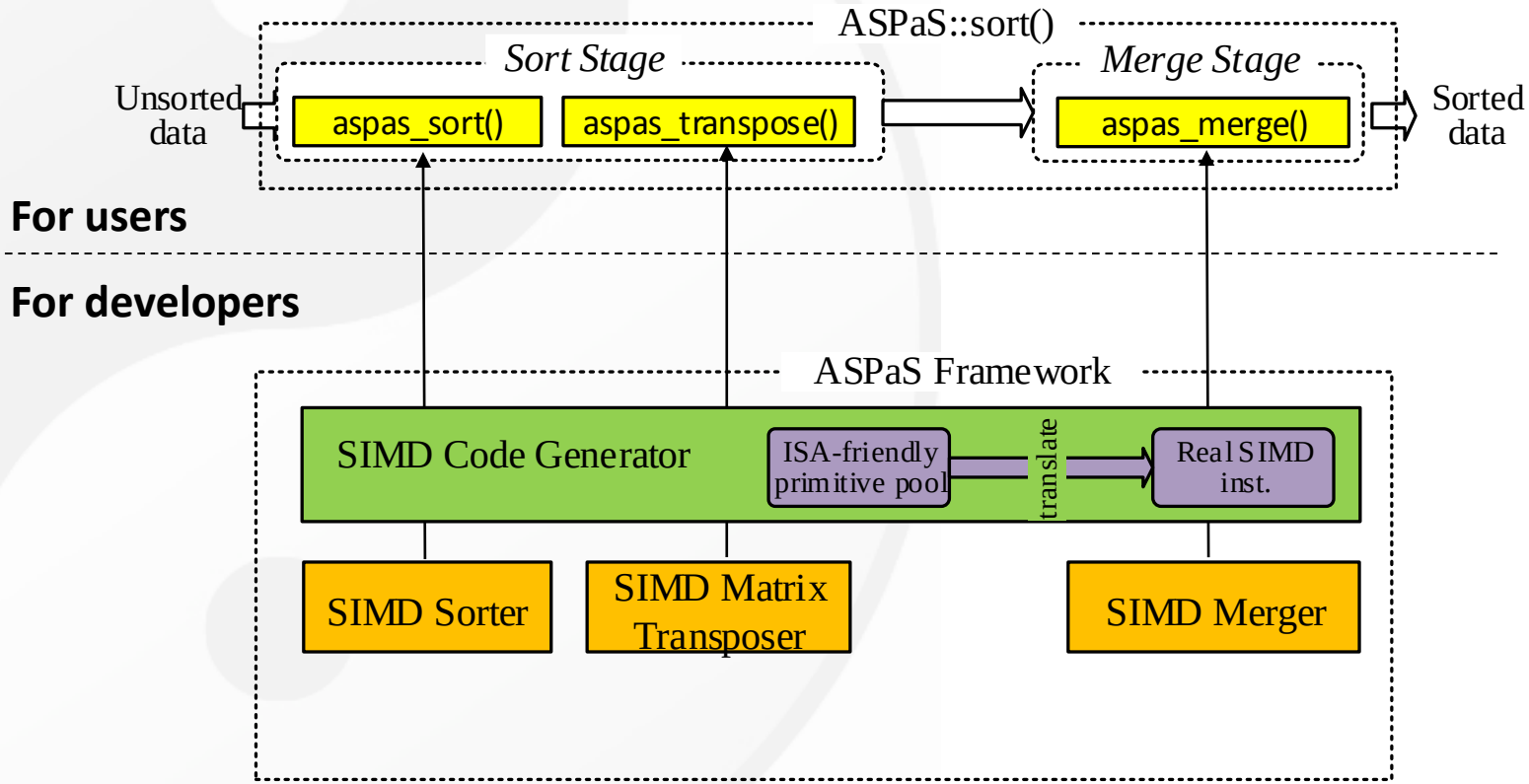

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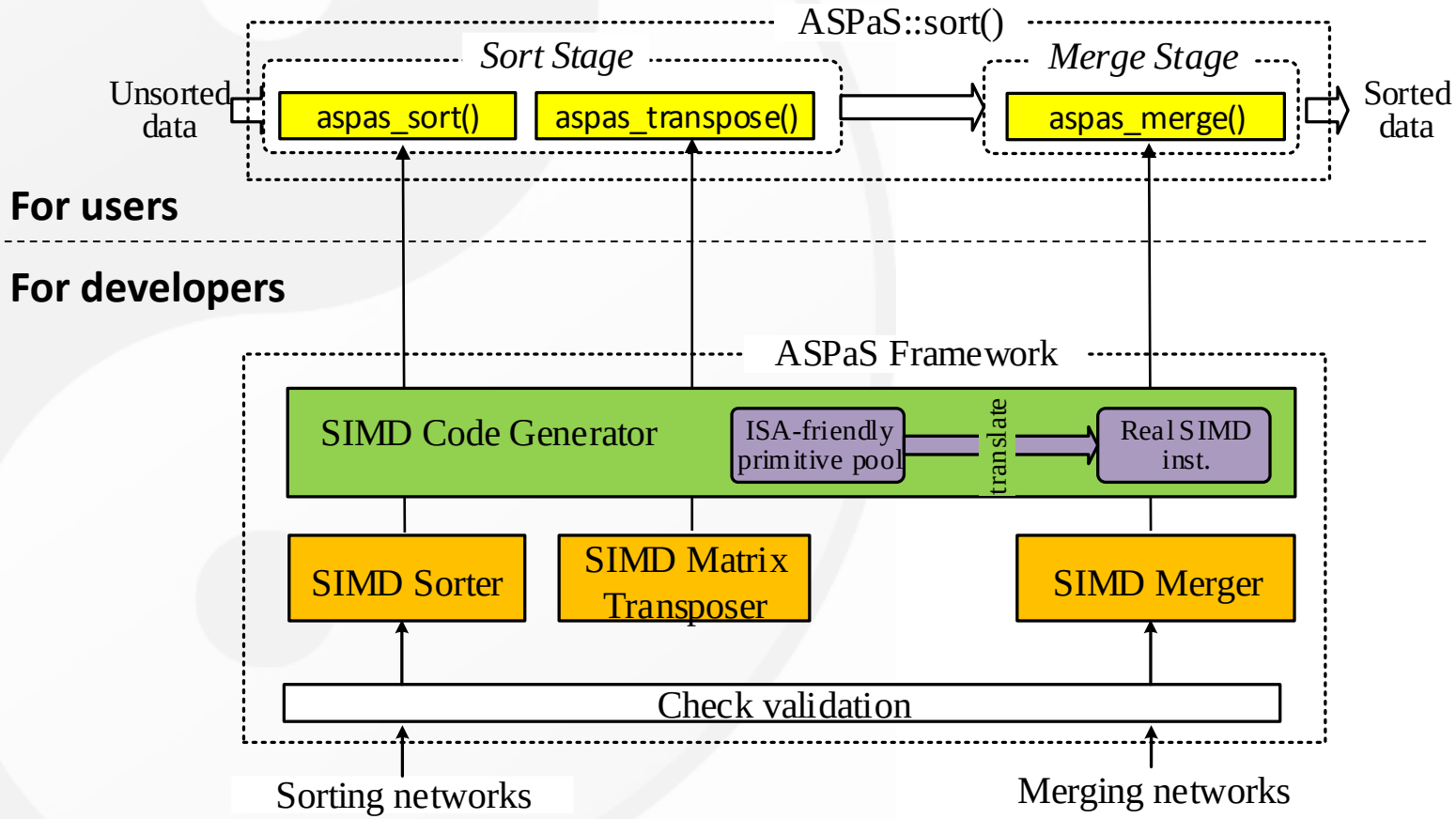

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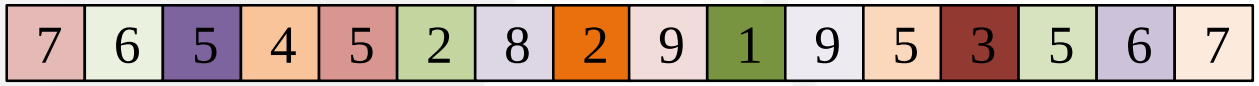

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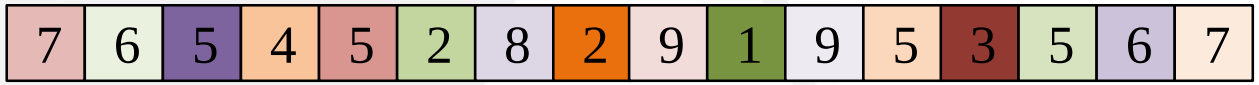

We'd like to sort this array in the SIMD style.

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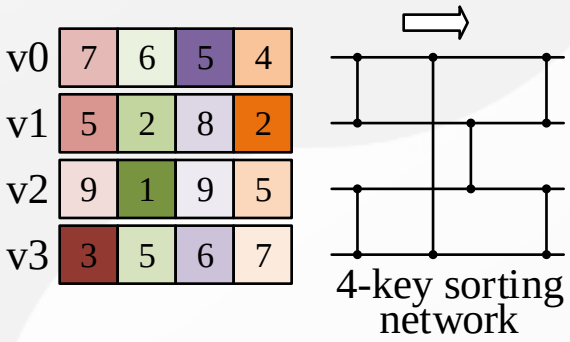

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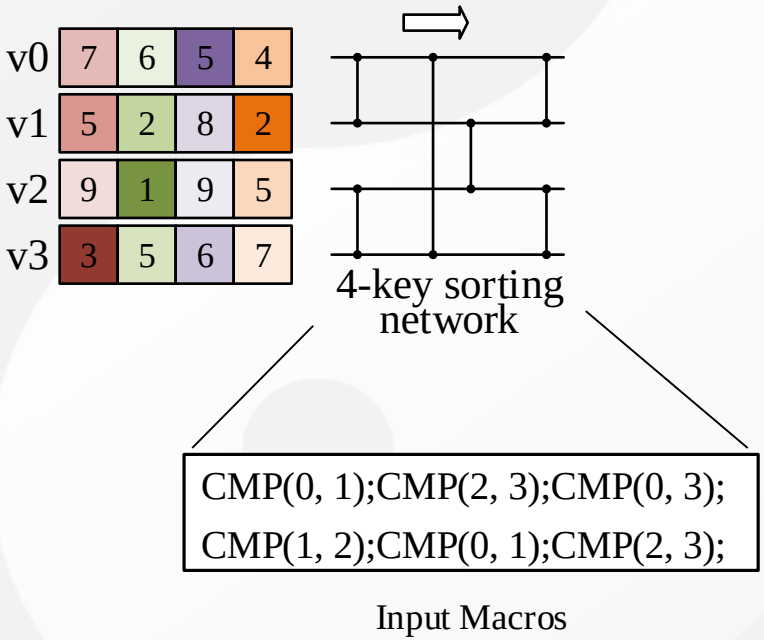

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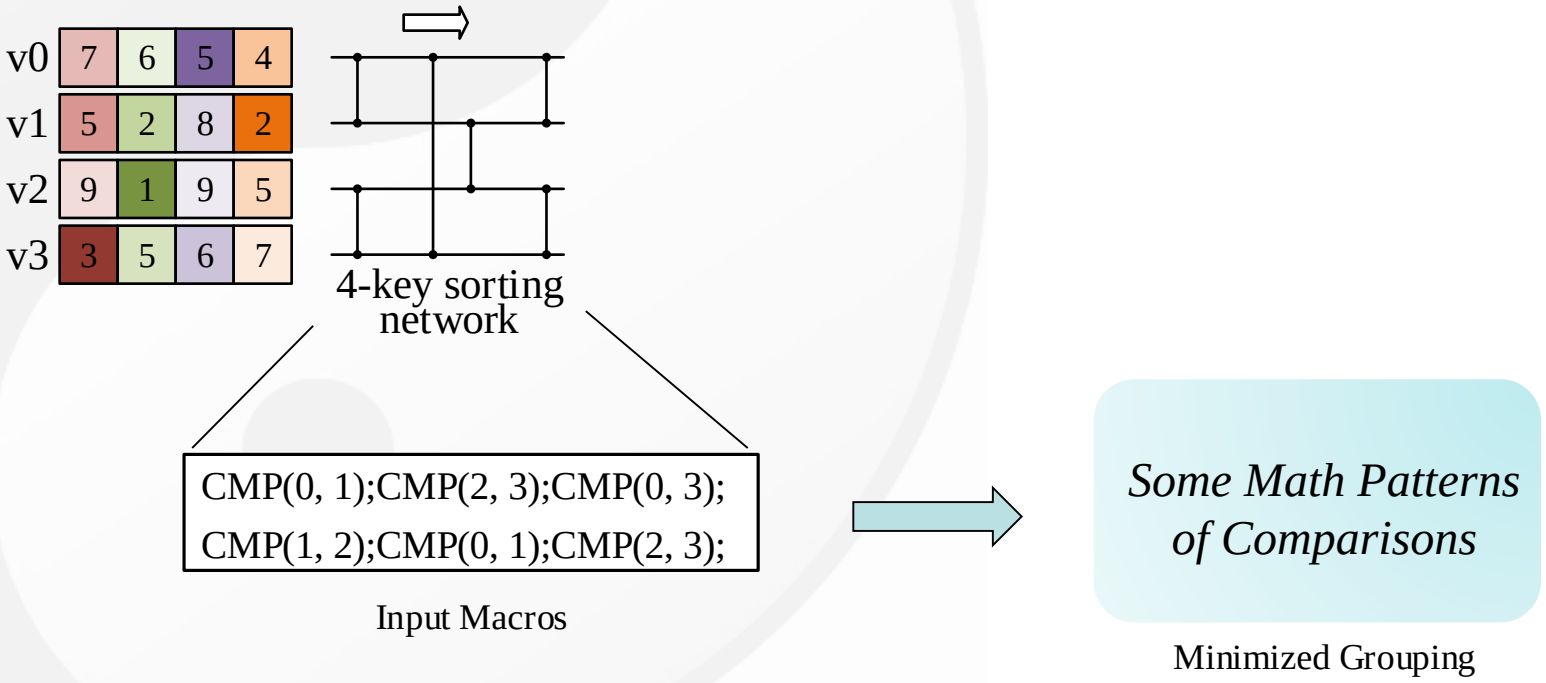
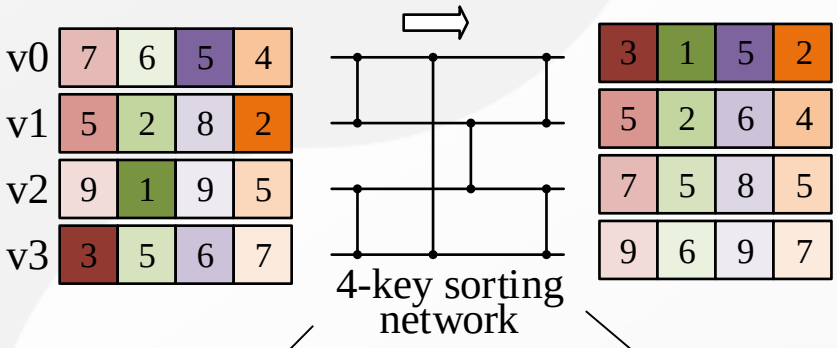


ASPaS Framework

- SIMD Sorter
  - Generate regrouped comparison patterns
  - Accept any kinds of sorting networks



CMP(0, 1);CMP(2, 3);CMP(0, 3);
CMP(1, 2);CMP(0, 1);CMP(2, 3);

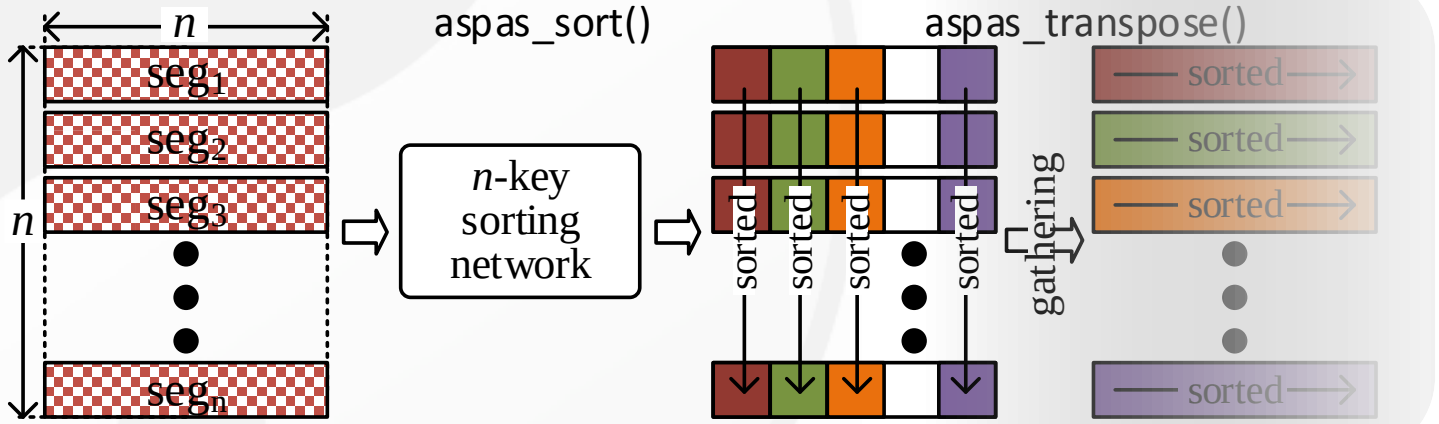
Input Macros

Some Math Patterns of Comparisons

Minimized Grouping

ASPaS Framework

- SIMD Transposer
  - Why need the transpose?



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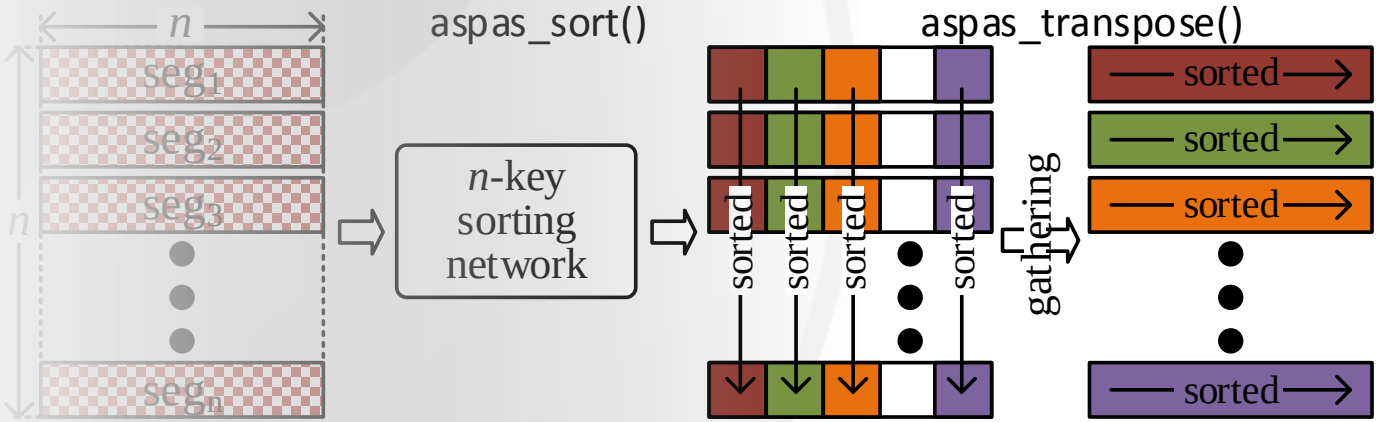

ASPaS Framework

- SIMD Transposer
  - Generalize the patterns required in the in-register transpose

ASPaS Framework

- SIMD Transposer
  - Generalize the patterns required in the in-register transpose

v0	3	1	5	2
v1	5	2	6	4
v2	7	5	8	5
v3	9	6	9	7

ASPaS Framework

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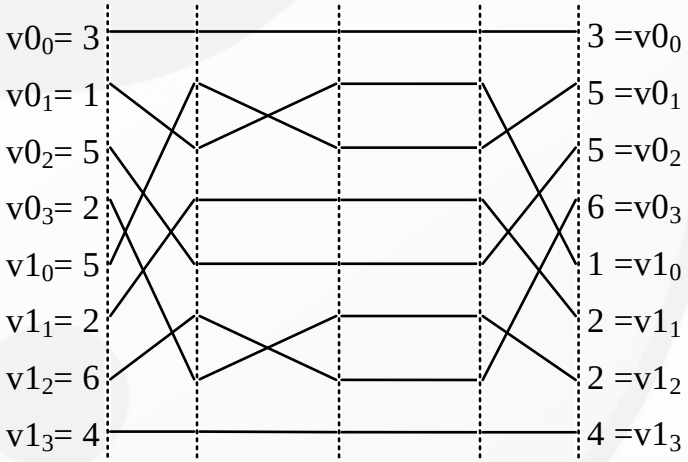

Same pattern applies on v2 and v3

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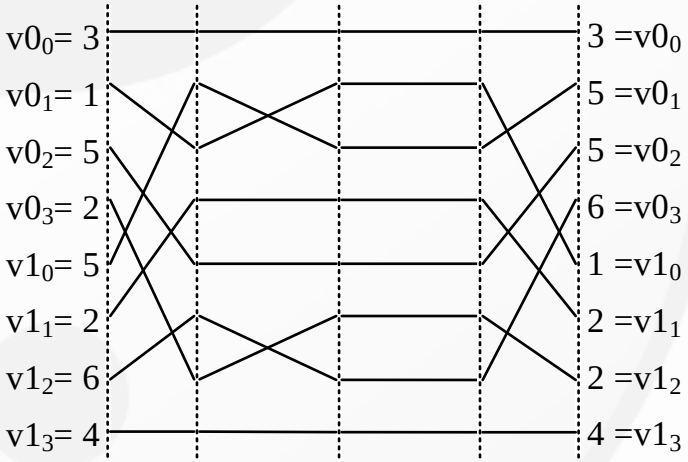

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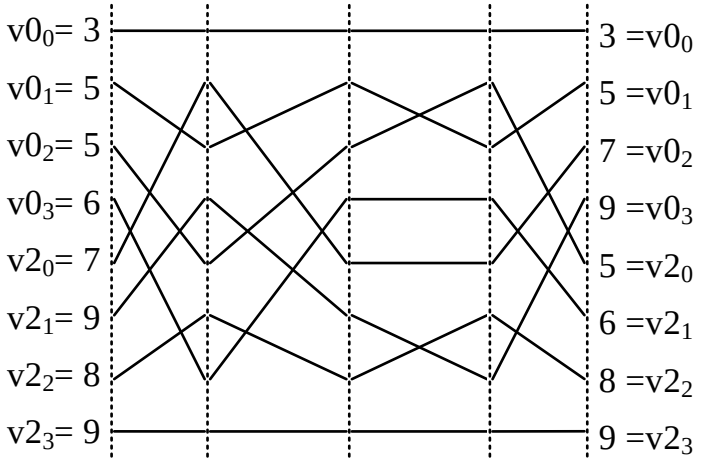

Same pattern applies on v1 and v3

ASPaS Framework

- SIMD Transposer
  - Generalize the patterns required in the in-register transpose

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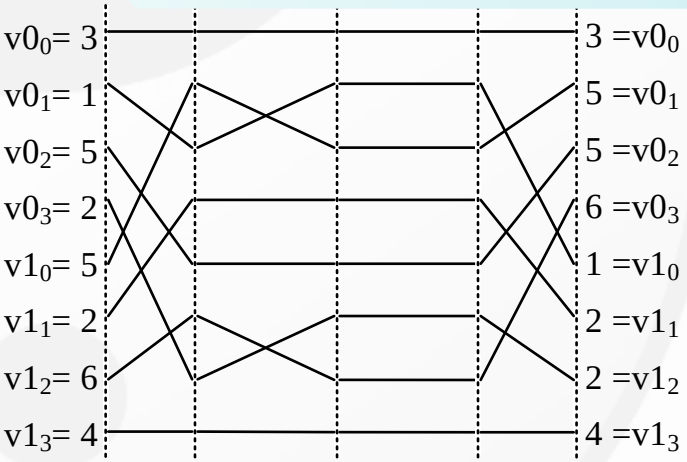
Some data-reordering patterns



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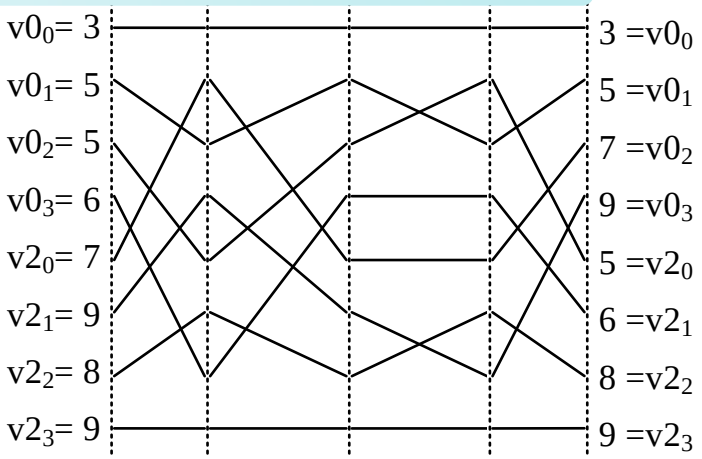

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ASPaS Framework

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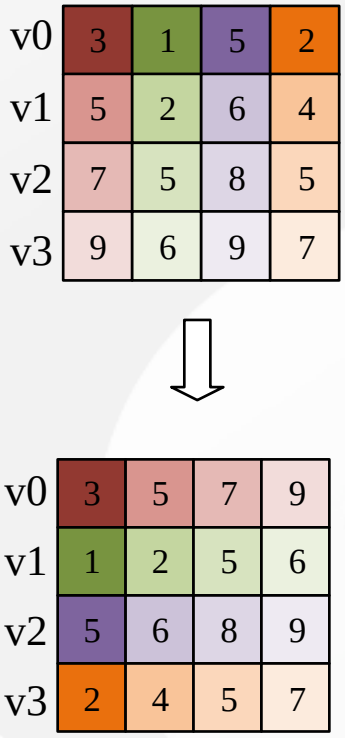
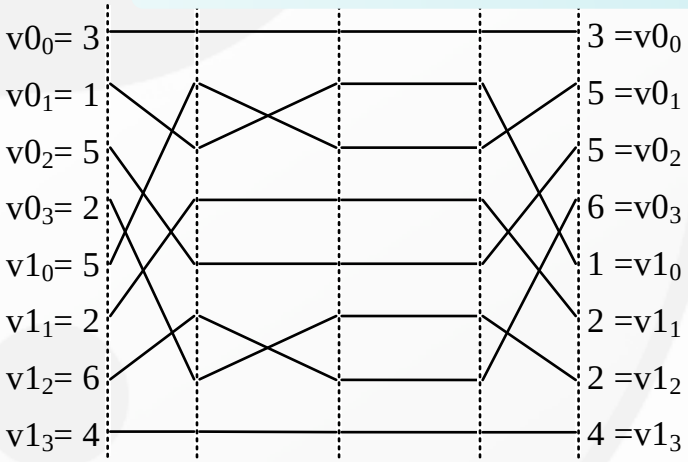


Some data-reordering patterns



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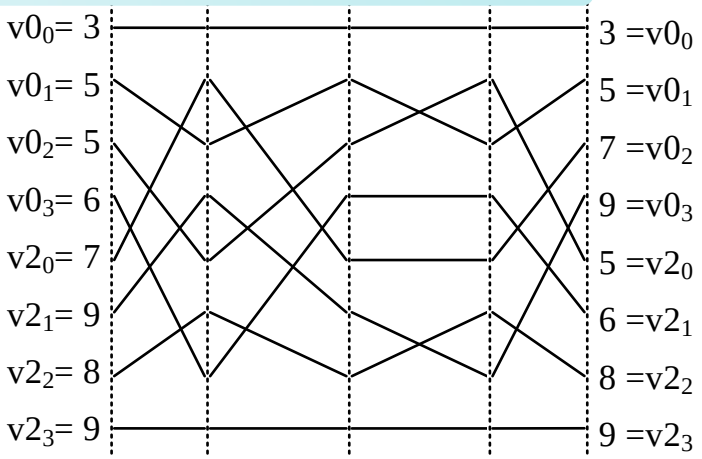

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ASPaS Framework

- SIMD Merger
  - Generalize the patterns required in the in-register merge

ASPaS Framework

- SIMD Merger
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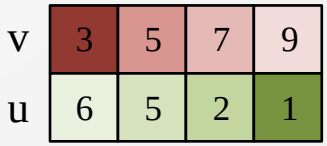
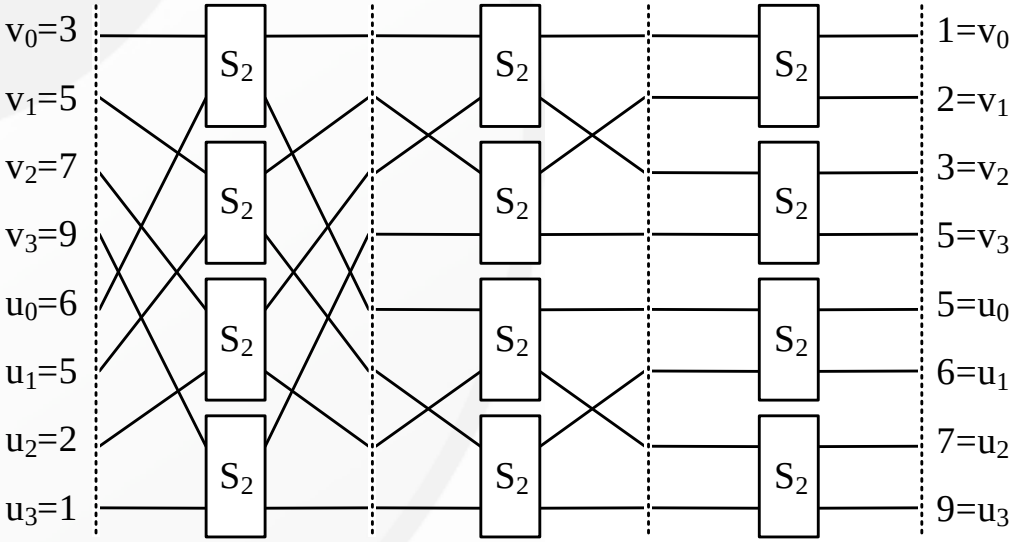


ASPaS Framework

- SIMD Merger
  - Generalize the patterns required in the in-register merge

v	3	5	7	9
u	6	5	2	1



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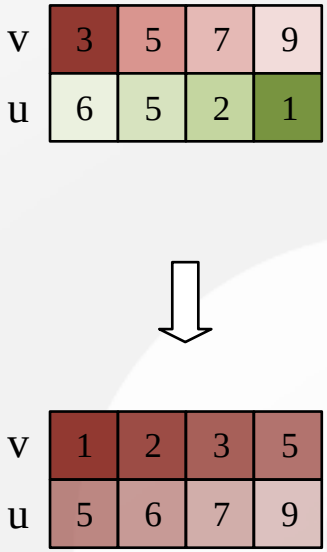

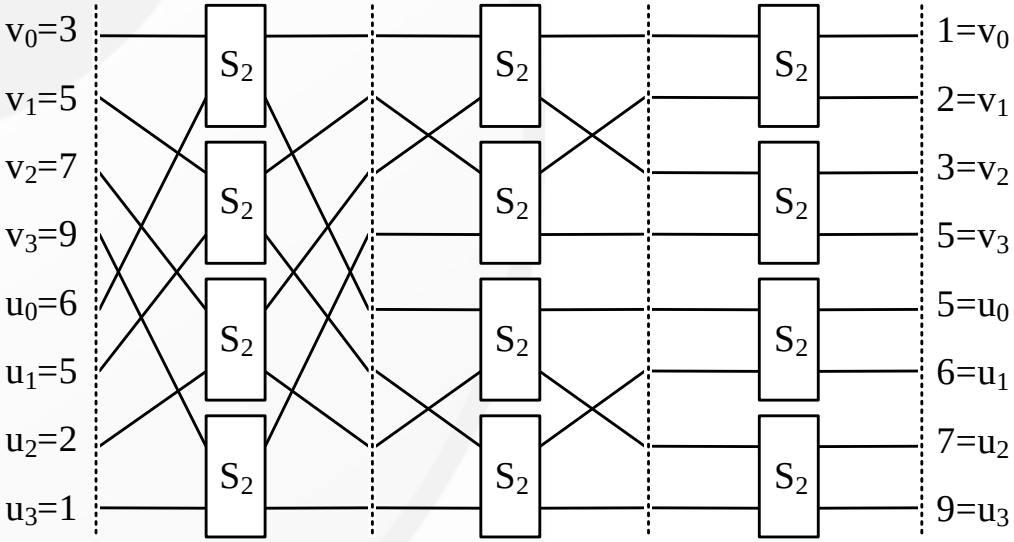

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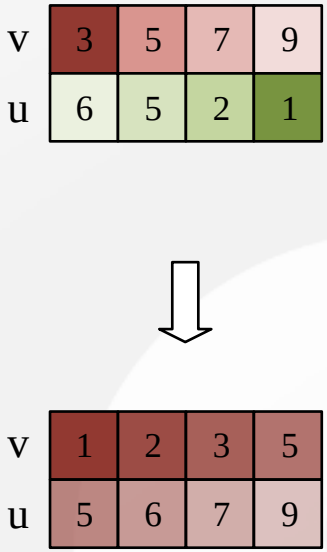

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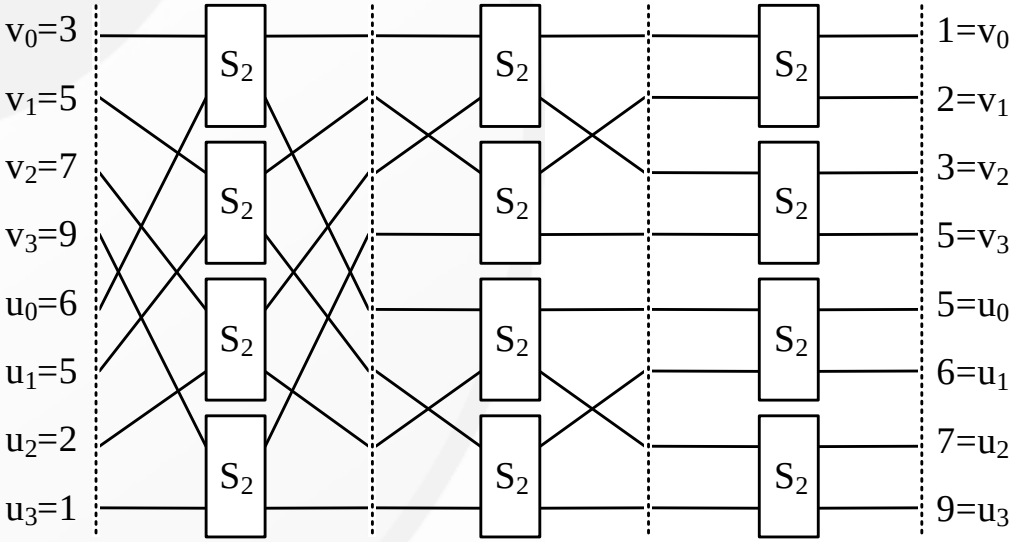

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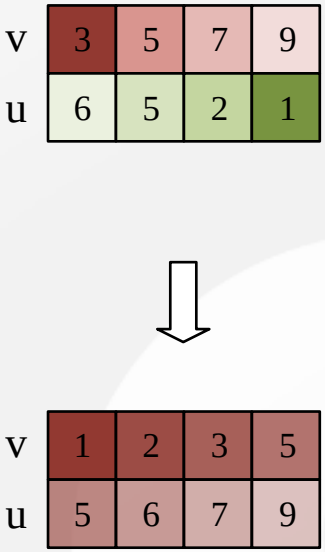

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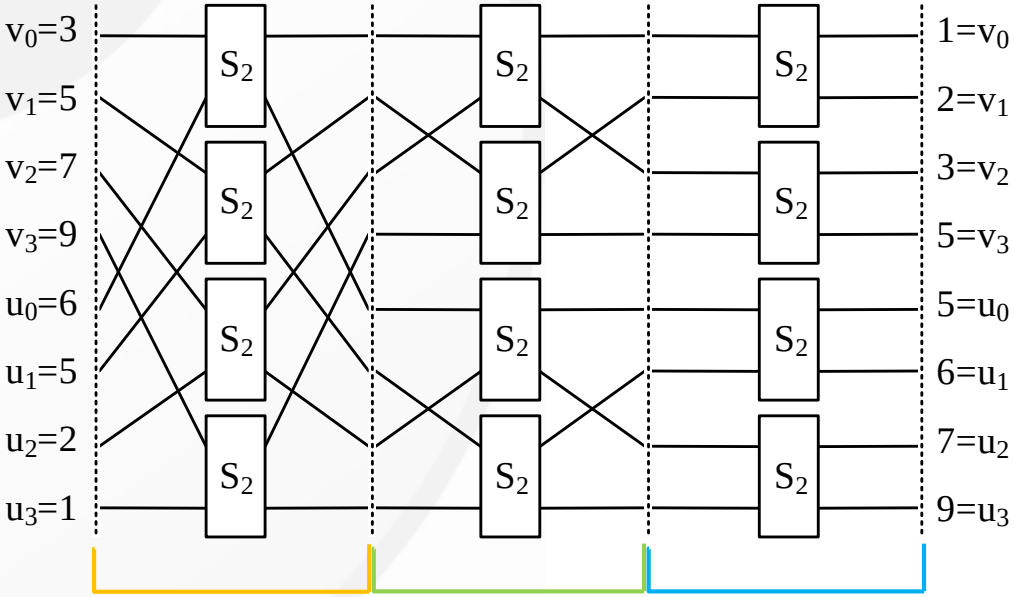

Inconsistent patterns

ASPaS Framework

- SIMD Code Generator
  - Sequence Building Algorithm

Target Vector

ASPaS Framework

- SIMD Code Generator
  - Sequence Building Algorithm

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Target Vector

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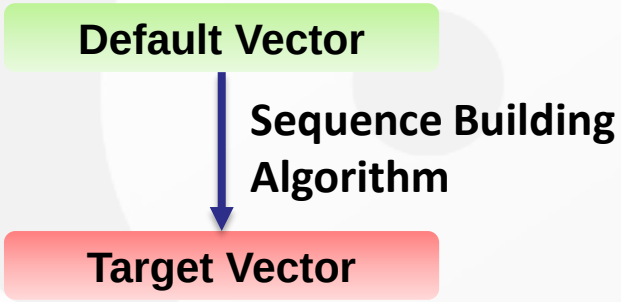

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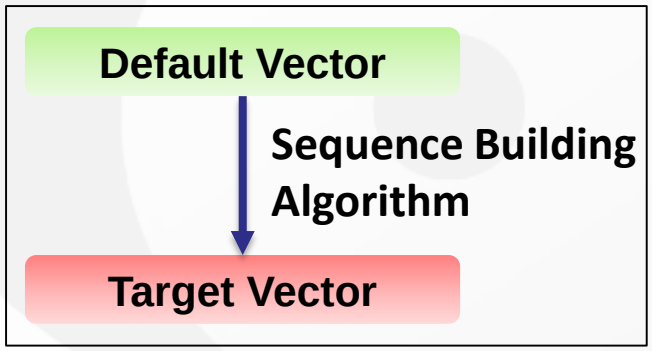

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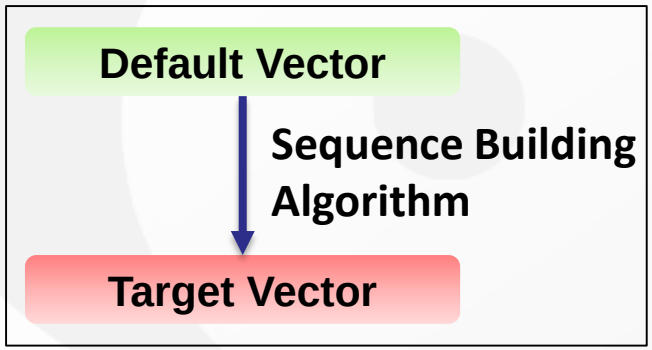
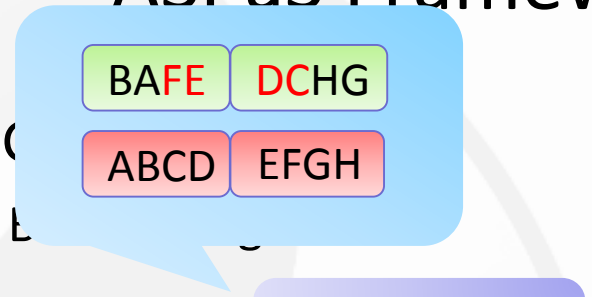
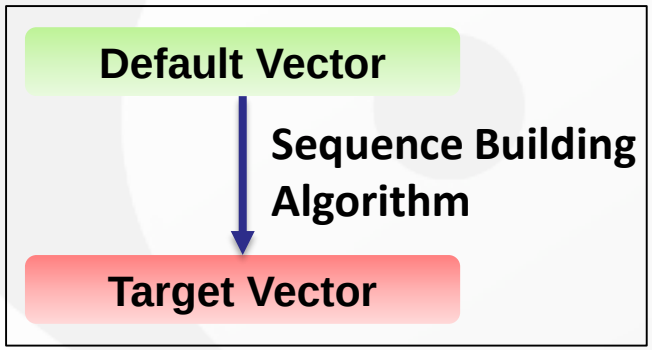


ASPaS Framework

- SIMD Code G
  - Sequence E





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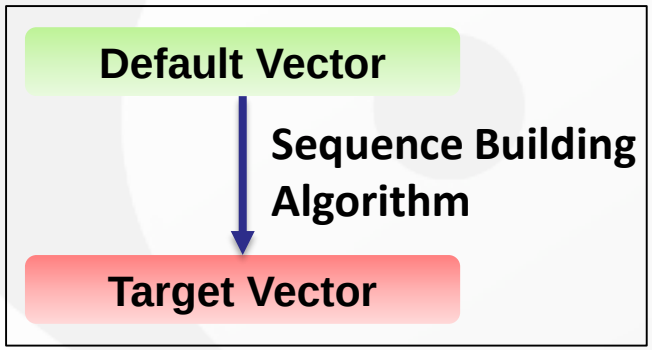

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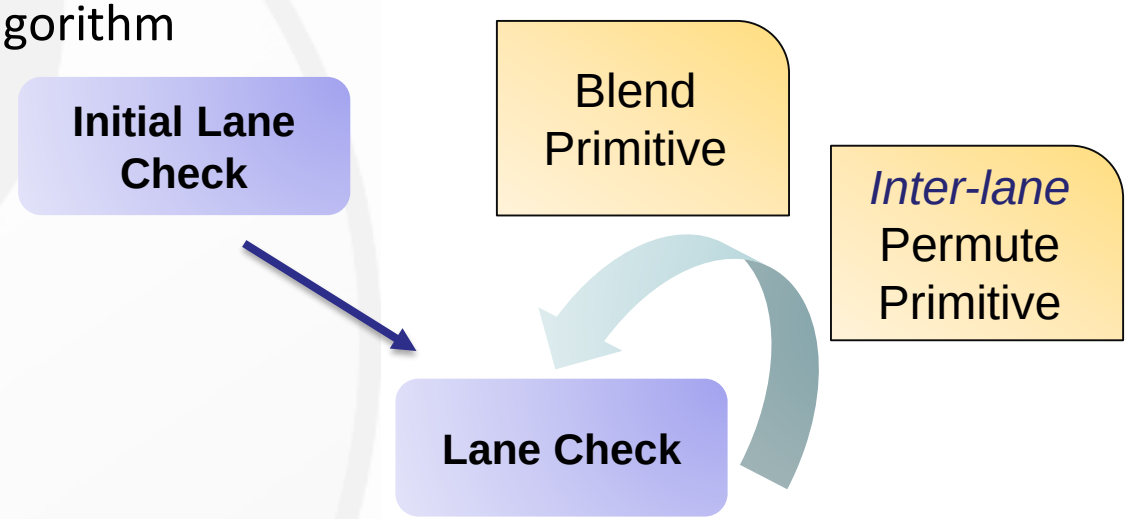

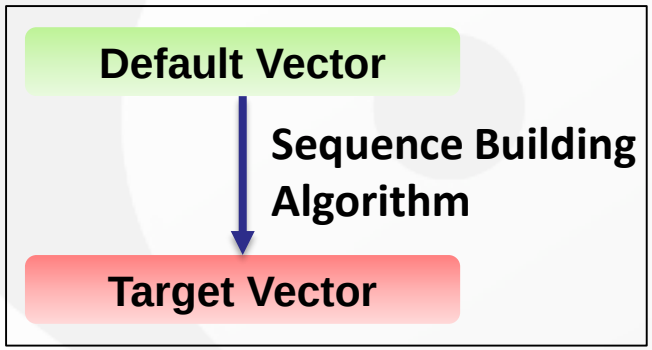

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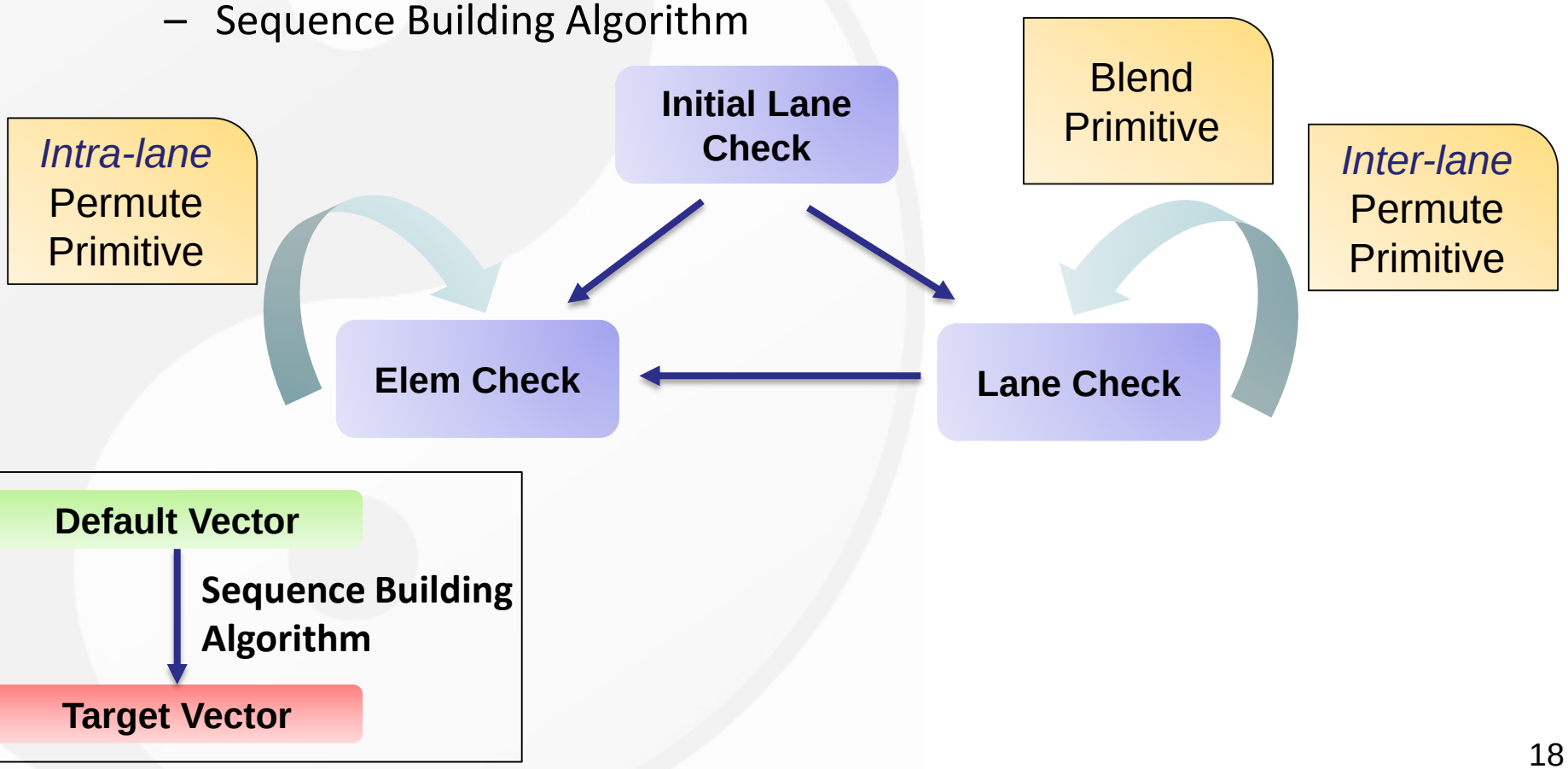

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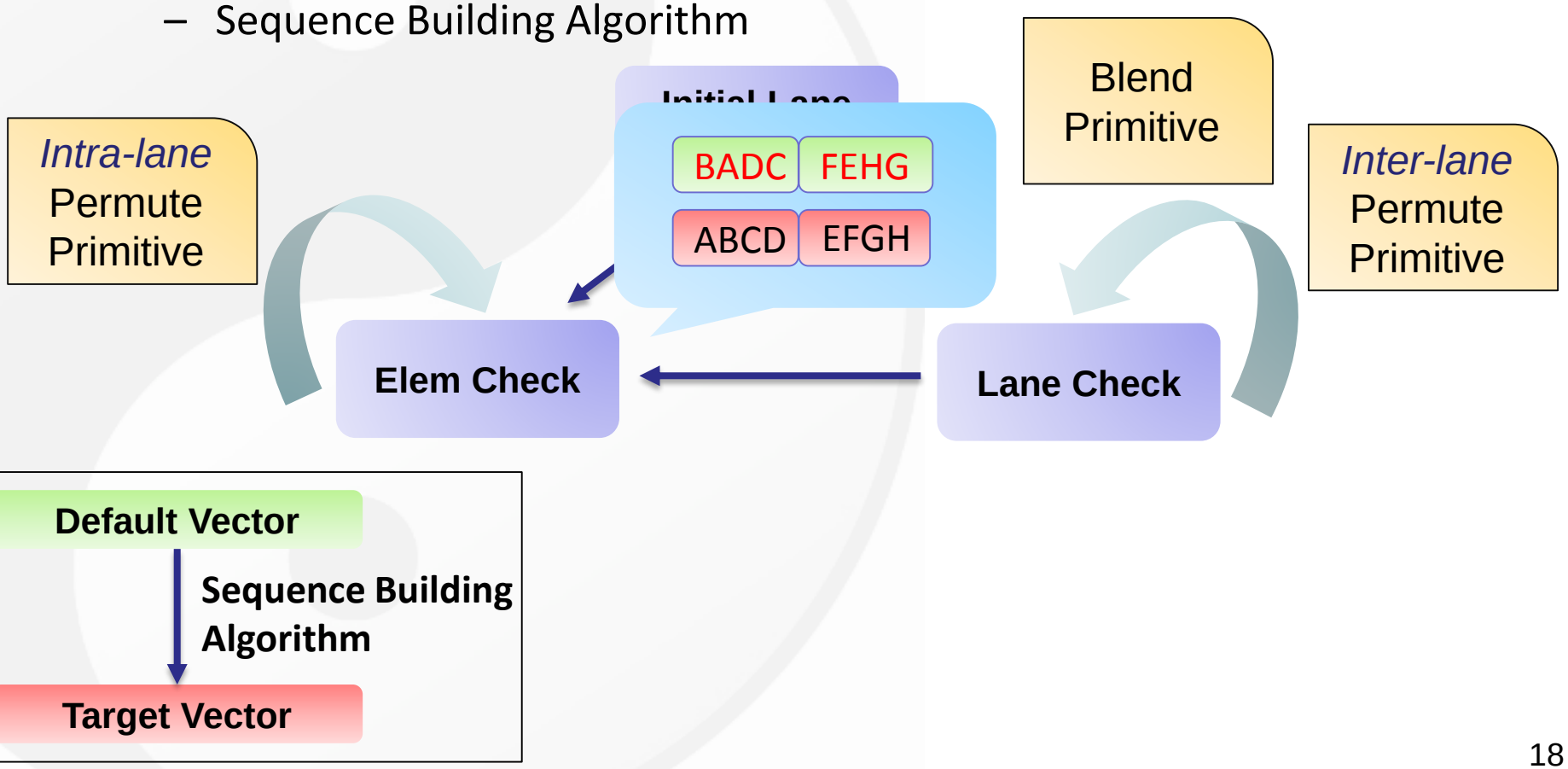

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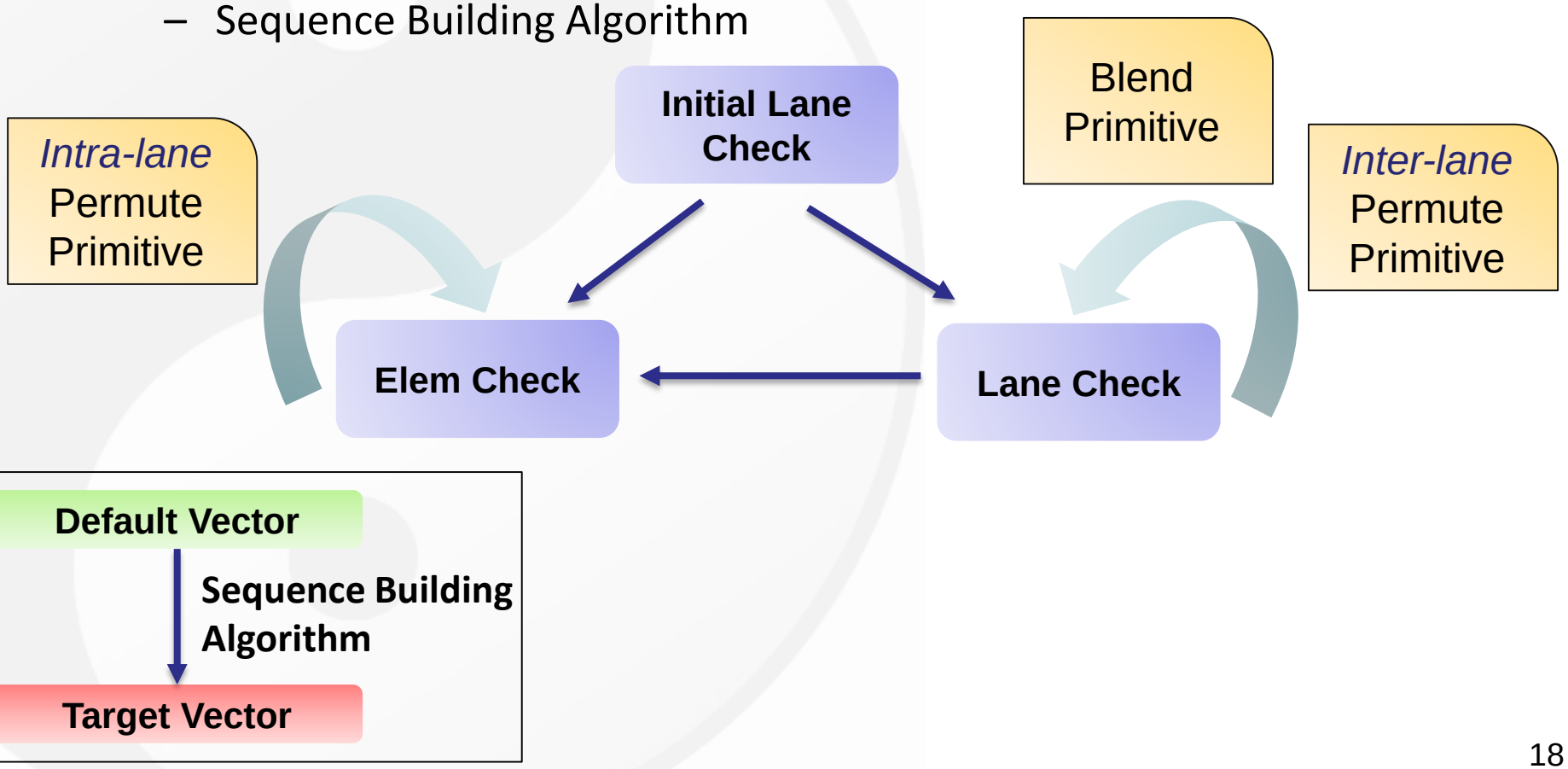

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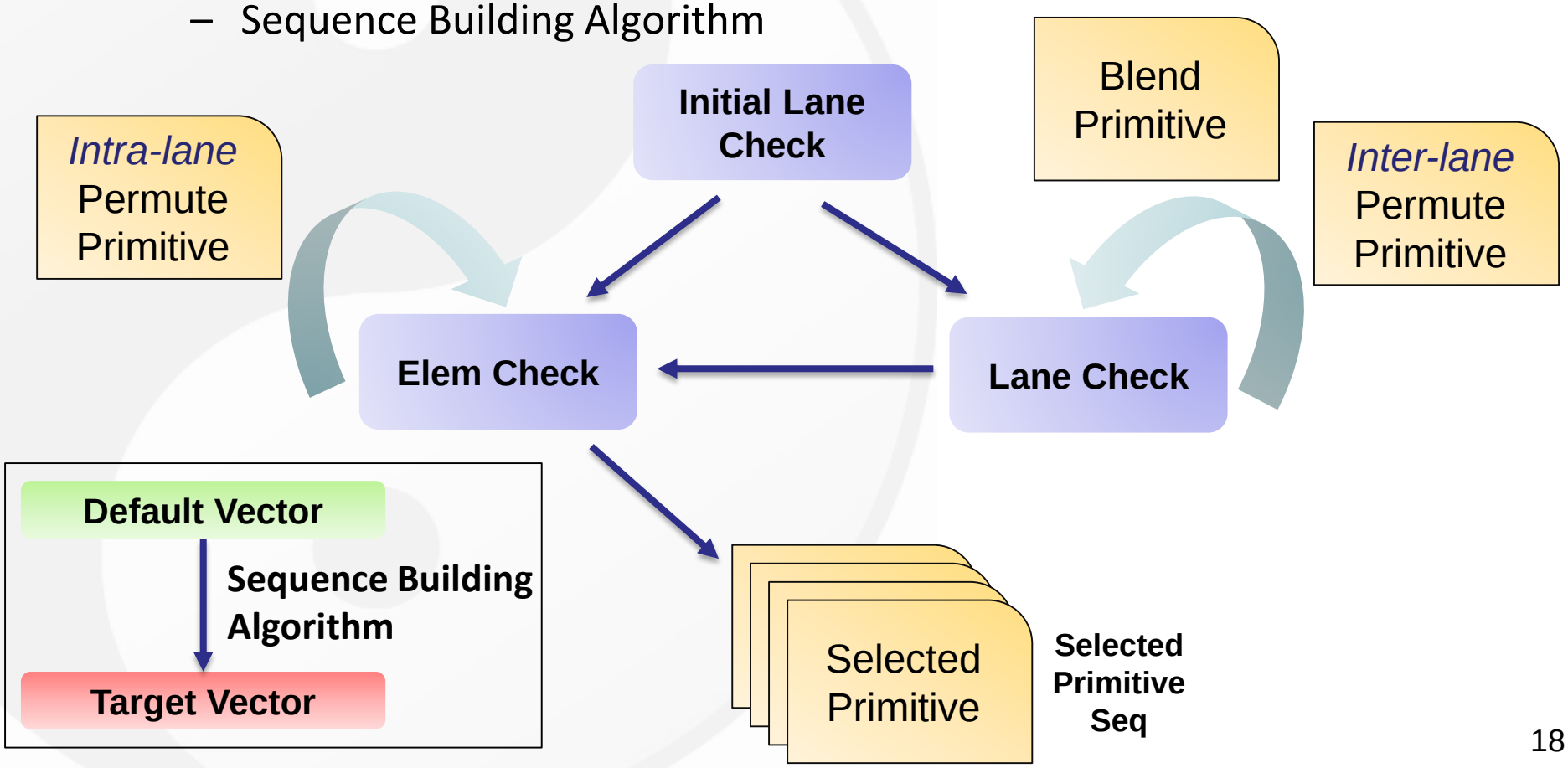

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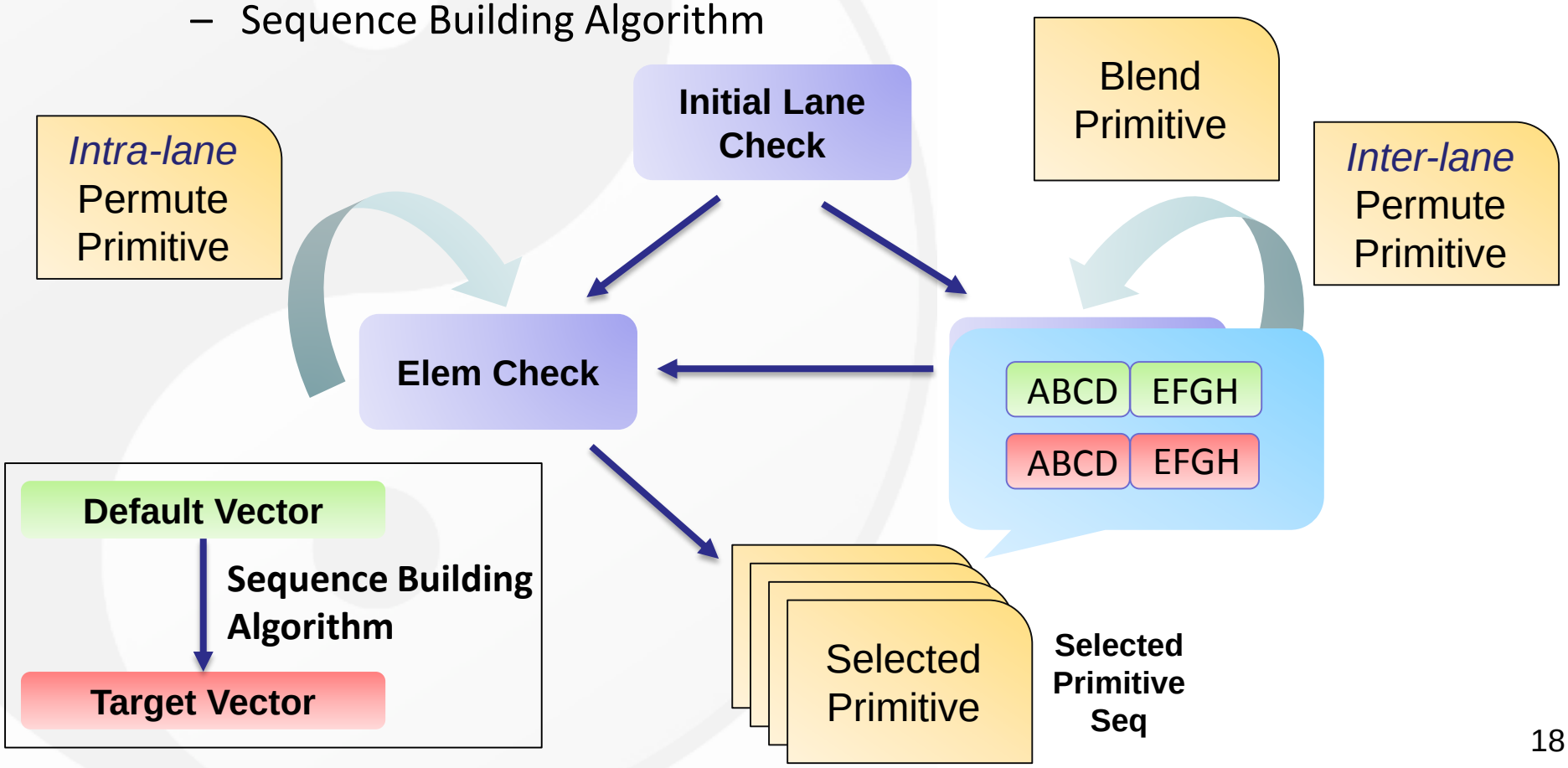

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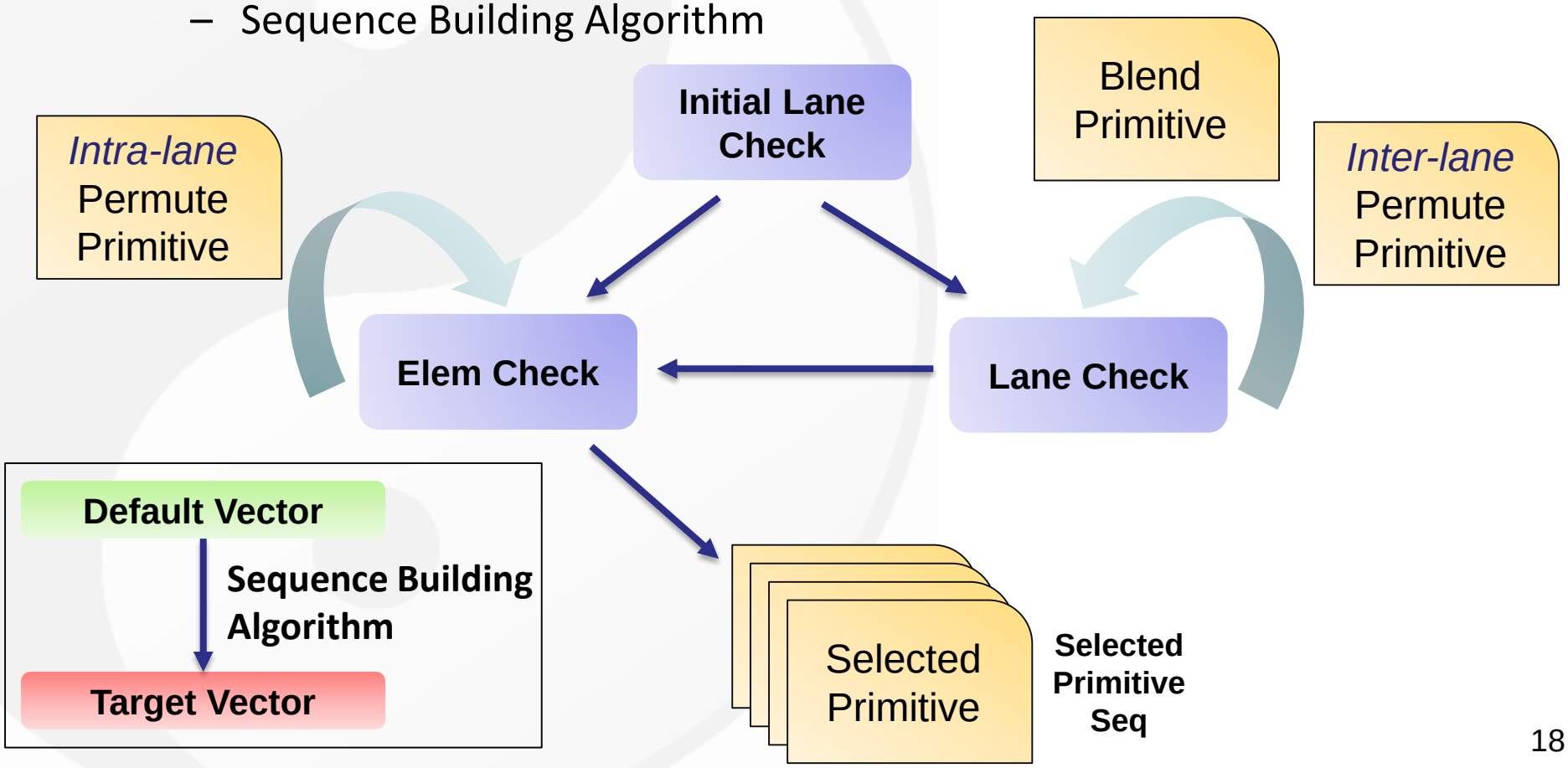

ASPaS Framework

- SIMD Code Generator
  - Translate: selected primitive sequence to real codes

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    - Intra-lane permute primitive => _mm512_shuffle
    - Inter-lane permute primitive => _mm512_permute4f128
    - Blend primitive => mask integrated to bond shuffle/permute instructions

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    - Blend primitive => mask integrated to bond shuffle/permute instructions
  - Towards TLP
    - Threads sort their own parts (aspas::sort())
    - Half of them merge the adjacent parts (aspas::merge())
      - Continues until only one thread left

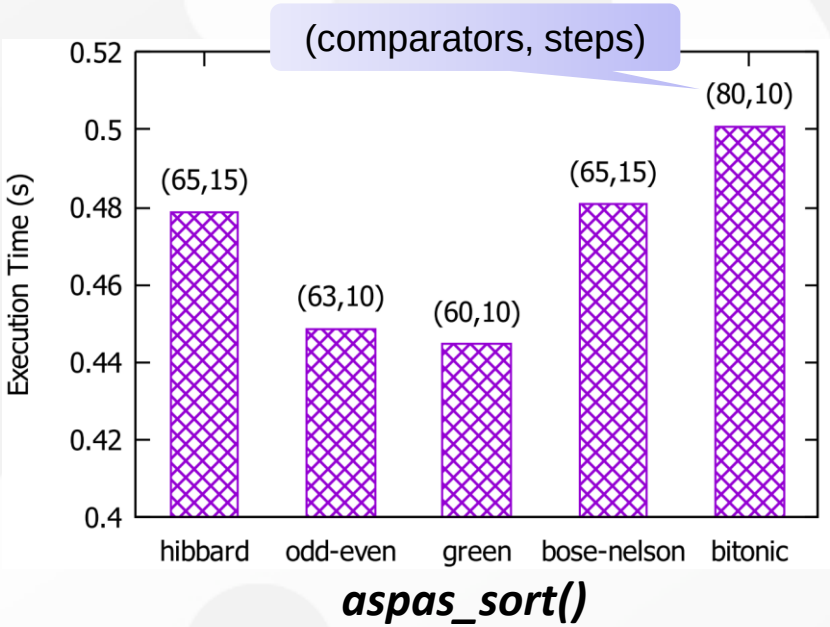
Evaluation & Discussion

- Experiment Setup

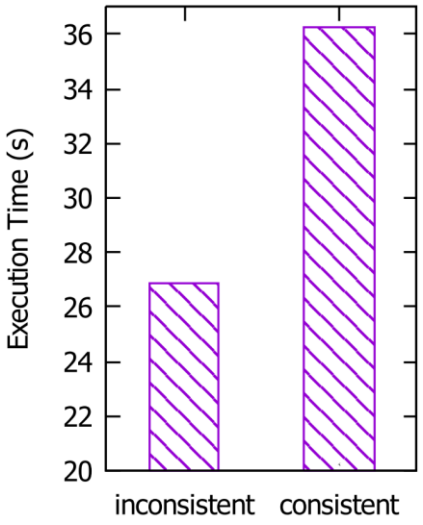
Parameter	Value
MIC	Intel Xeon Phi 5110P
Code Name	Knights Corner
# of Cores	60
Clock Rate	1.05 GHz
L1/L2 Cache	32 KB/ 512 KB
Memory	8 GB GDDR5
Compiler	icpc 13.0.1
Compiler Options	-mmic -O3
Random Number Range	[0, DATA_SIZE]

Evaluation & Discussion

- Performance of Different Sorting Networks



aspas_sort()



aspas_merge()

Evaluation & Discussion

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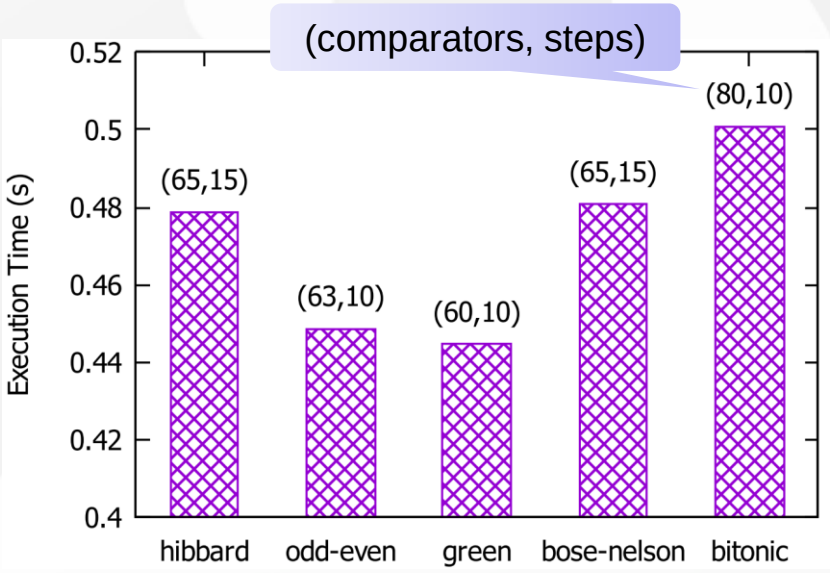

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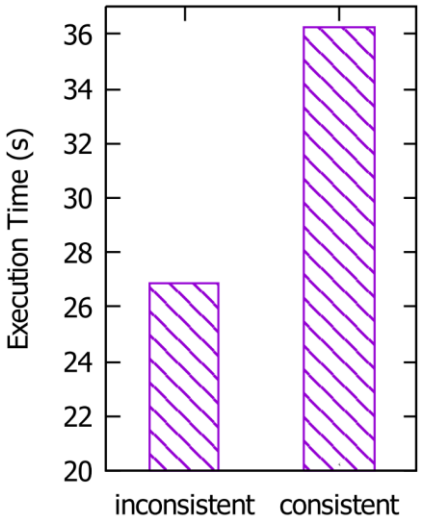

aspas_merge()

  - ASPaS_sort(): More comparators, worse performance

Evaluation & Discussion

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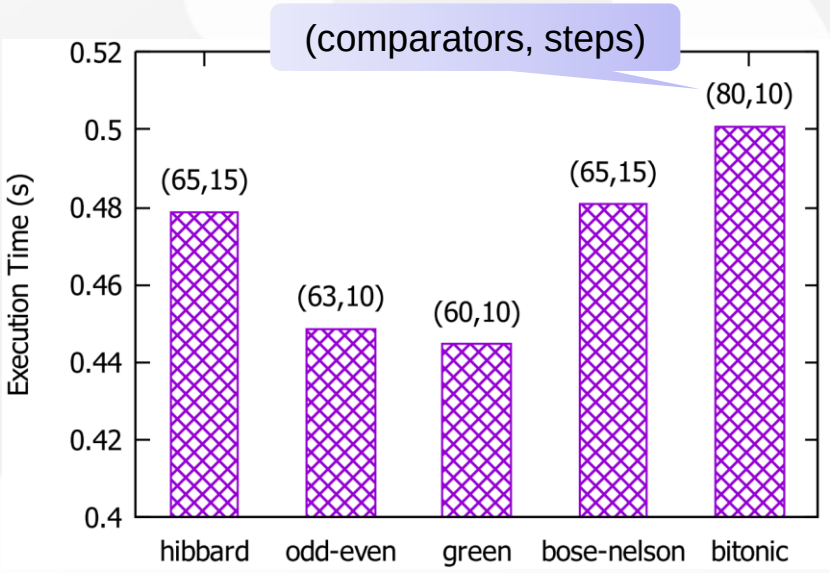

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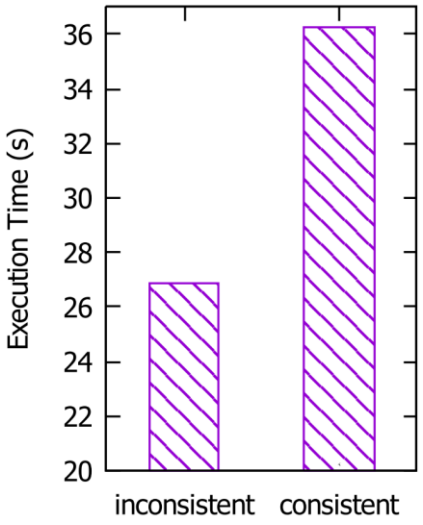
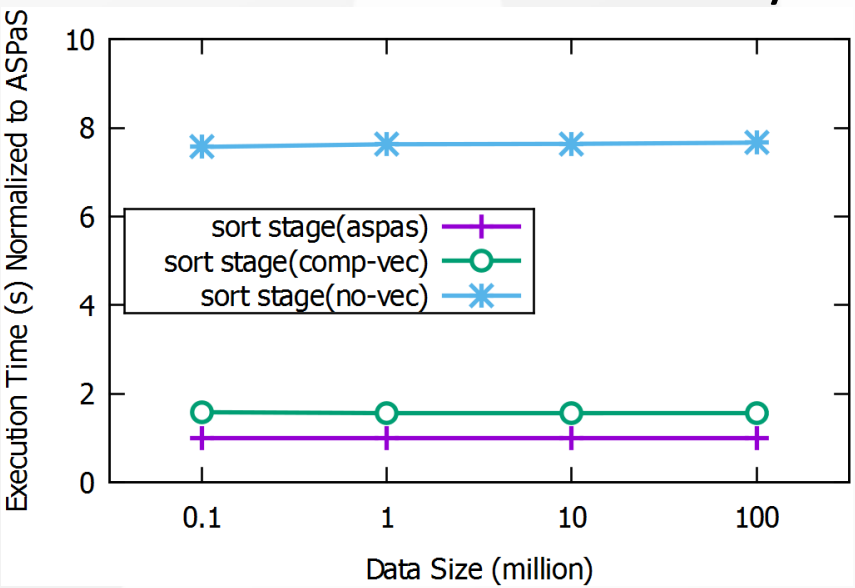


aspas_merge()

  - ASPaS_sort(): More comparators, worse performance
  - ASPaS_merge(): “Consistent” variant consists of the SIMD-unfriendly interleaving data-reordering

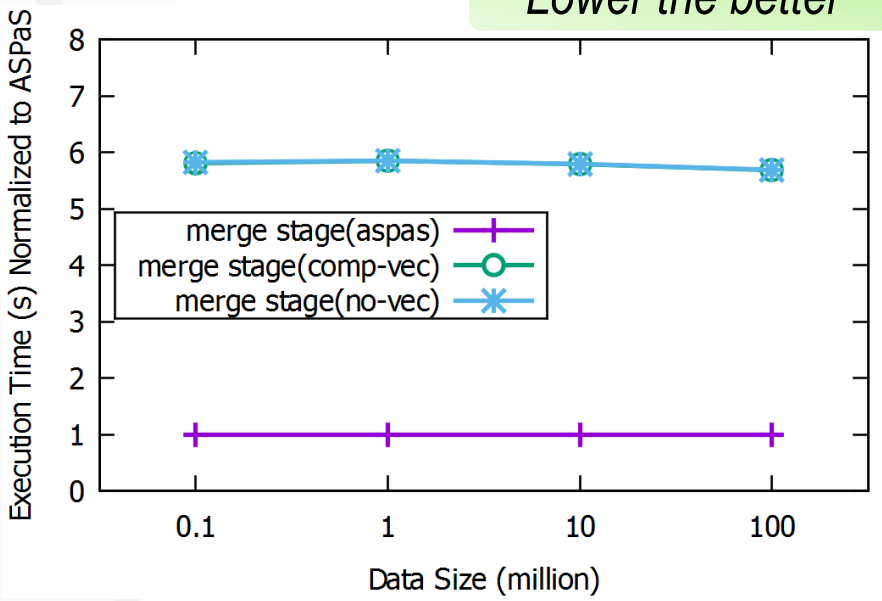
Evaluation & Discussion

- Vectorization Efficiency



Sort stage

Lower the better

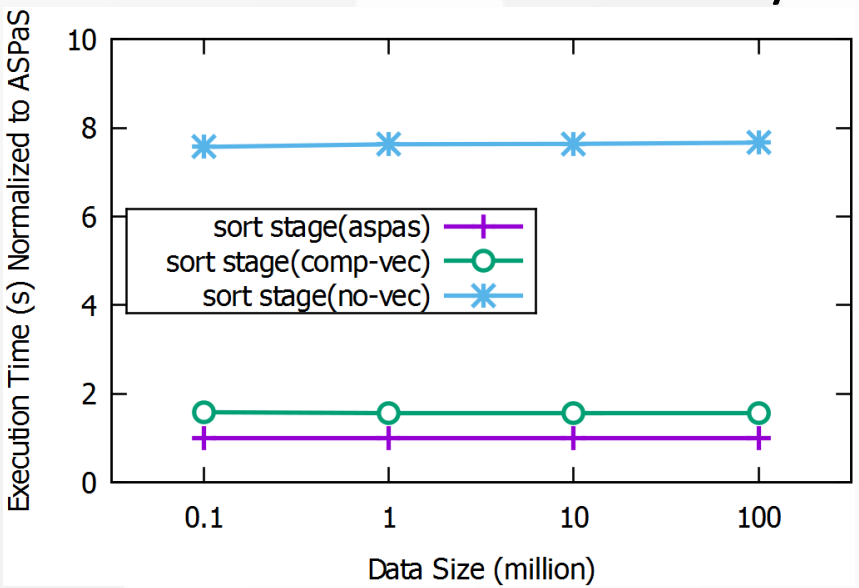


Merge stage

Evaluation & Discussion

- Vectorization Efficiency

Lower the better



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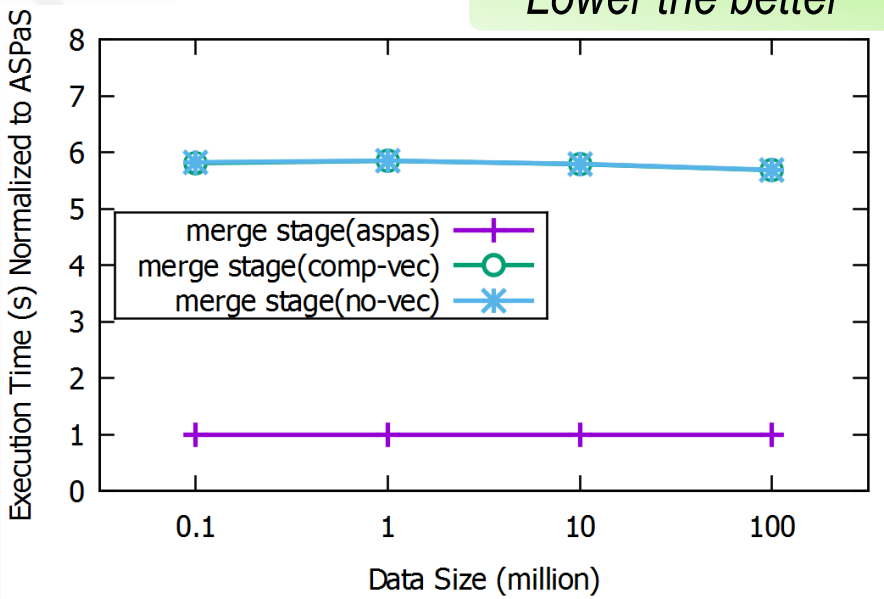

Merge stage

- Sort stage: ASPaS still can outperform the auto-vec version, thanks to its contiguous memory access

Evaluation & Discussion

- Vectorization Efficiency

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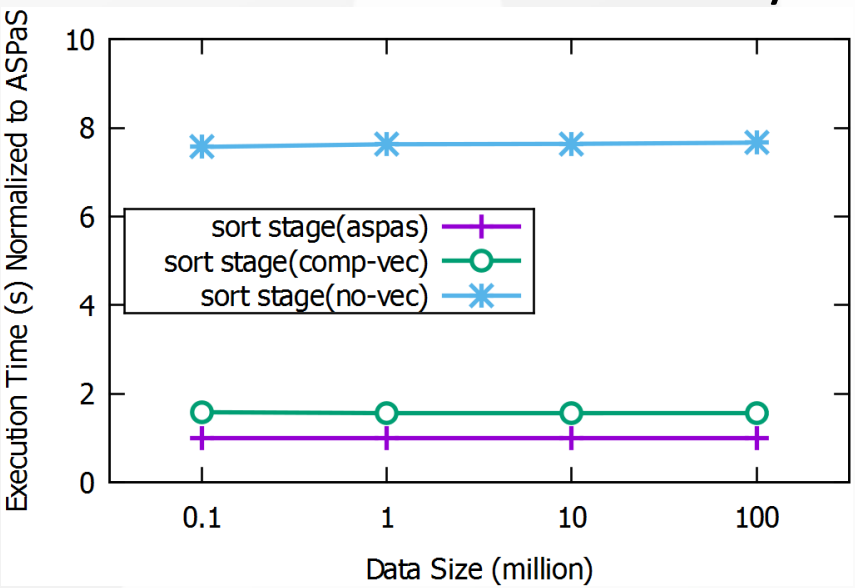

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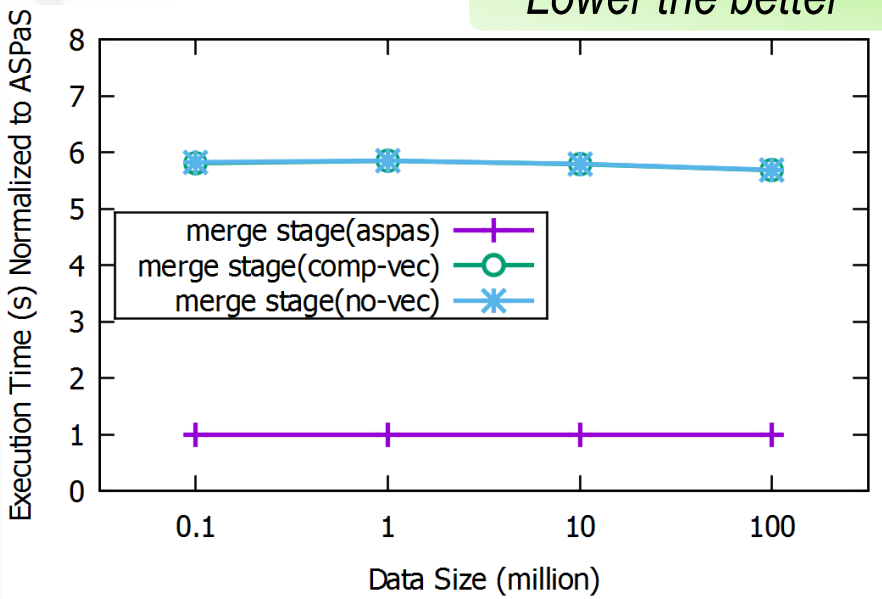


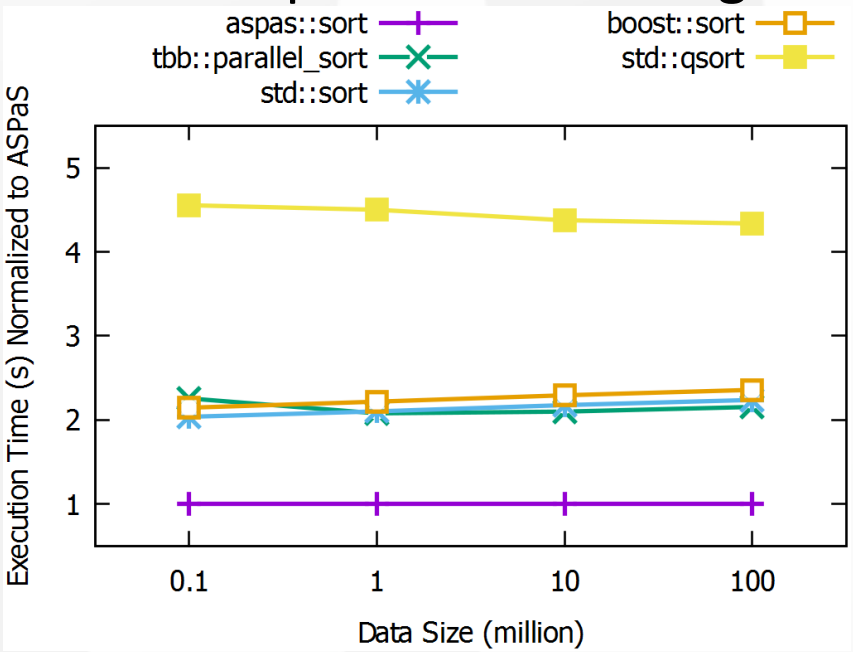
Merge stage

- Sort stage: ASPaS still can outperform the auto-vec version, thanks to its contiguous memory access
- Merge stage: the complex data dependency prevents the compiler from auto-vectorizing the loops

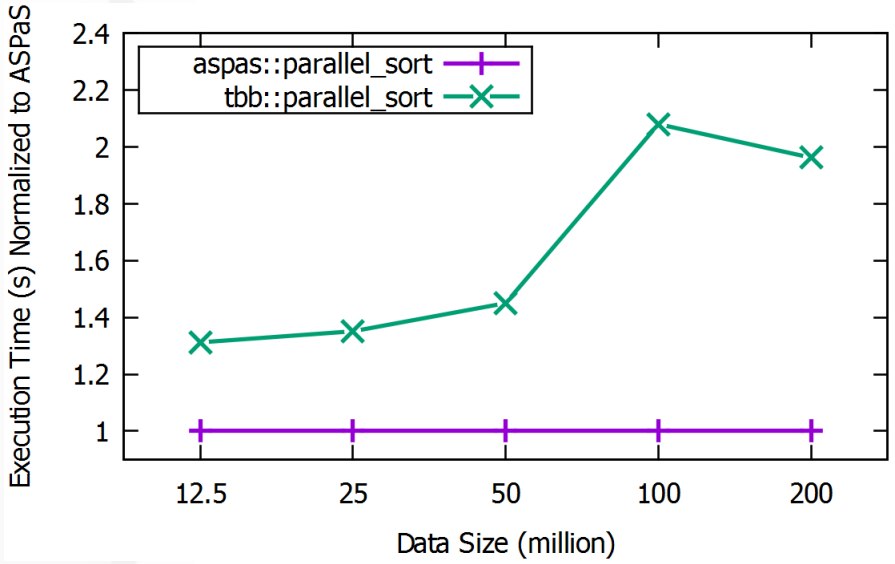
Evaluation & Discussion

- Comparison to Sorting from Libraries

Lower the better



Single-threaded sorts

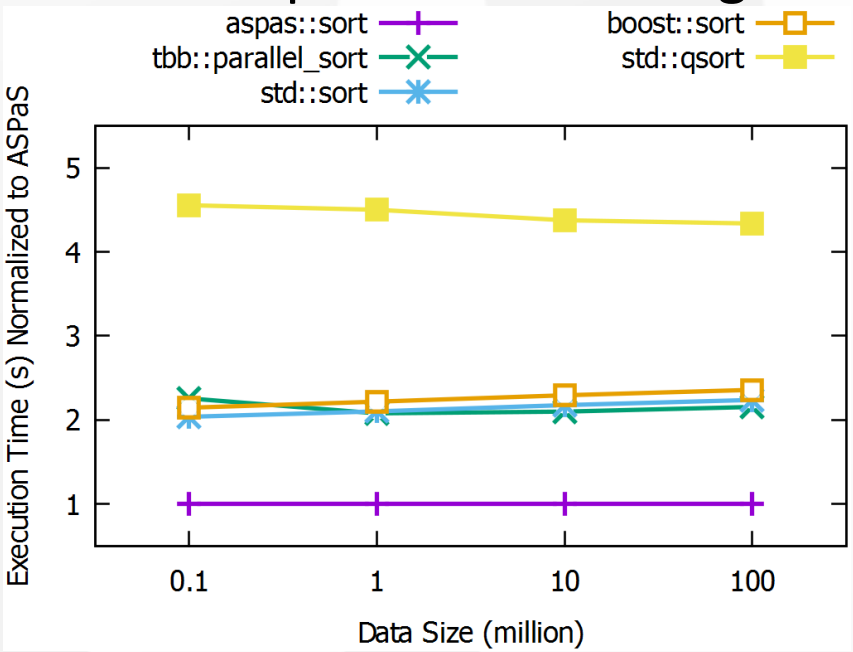


Multi-threaded sorts

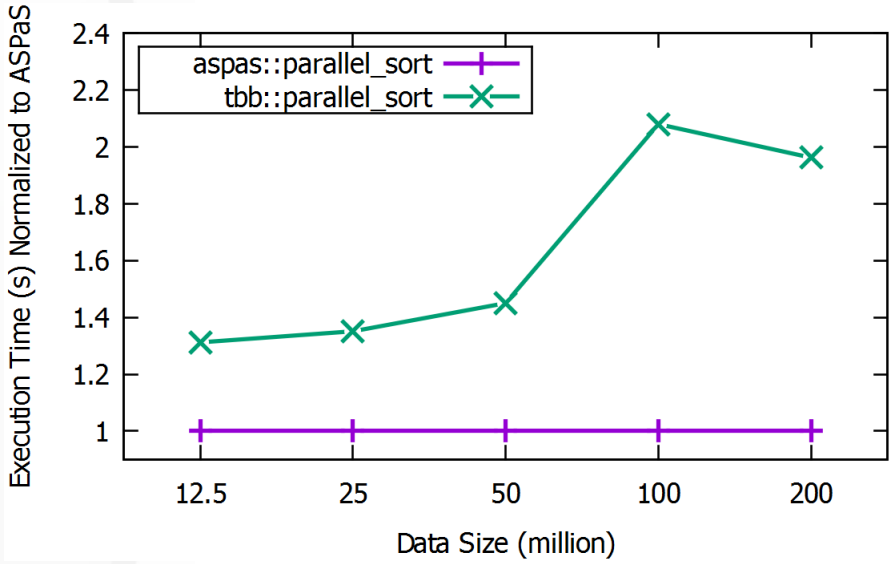
Evaluation & Discussion

- Comparison to Sorting from Libraries

Lower the better



Single-threaded sorts



Multi-threaded sorts

- ASPaS sort outperforms other sorting tools from widely-used libraries

Conclusion

- ASPaS: a framework for the Automatic SIMDization of Parallel Sorting code generation
  - Formalizes the data-reordering operations
  - Fast and efficiently build the real instruction sequences
  - Can be applied to CPU as well
- Various parallel sorting codes generated with ASPaS
  - Significant vectorization efficiency
  - Can outperform tools from STL, Boost, and Intel TBB

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THANK YOU!

Paper in ACM's ICS'15 and http://synergy.cs.vt.edu

Backup

- Portability
  - Easily ported to other x-86 multi-core CPU architectures
  - Only need to change the part of "Translate: primitives to real codes" in the SIMD Code Generator
    - Permute primitives => _mm256_shuffle/permute2f128
    - Blend primitives => e.g. _mm256_unpacklo/unpackhi